UNIVERSITÉ PARIS 13

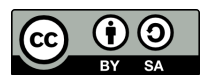
ESWEEK Tutorial

Sunday, 30th of September

Schedulability Analysis under Uncertainty using Formal Methods (part 2)

Étienne André and Giusppe Lipari

LIPN, Université Paris 13, CNRS, France

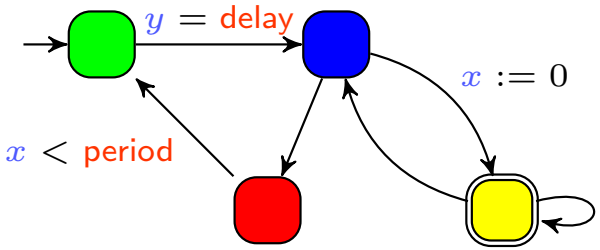


Outline

Model checking timed concurrent systems

- Use formal methods

[Baier and Katoen, 2008]



A model of the system

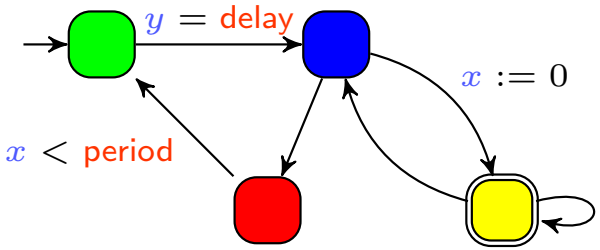
 is unreachable

A property to be satisfied

Model checking timed concurrent systems

- Use formal methods

[Baier and Katoen, 2008]



A model of the system

?

$\models$


is unreachable

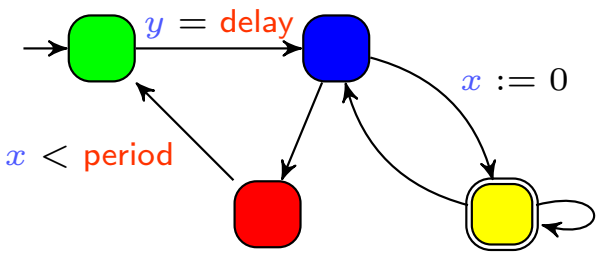
A property to be satisfied

- Question: does the model of the system satisfy the property?

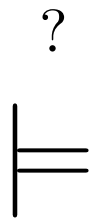
Model checking timed concurrent systems

- Use formal methods

[Baier and Katoen, 2008]



A model of the system



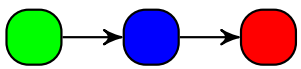

is unreachable

A property to be satisfied

- Question: does the model of the system satisfy the property?

Yes

No



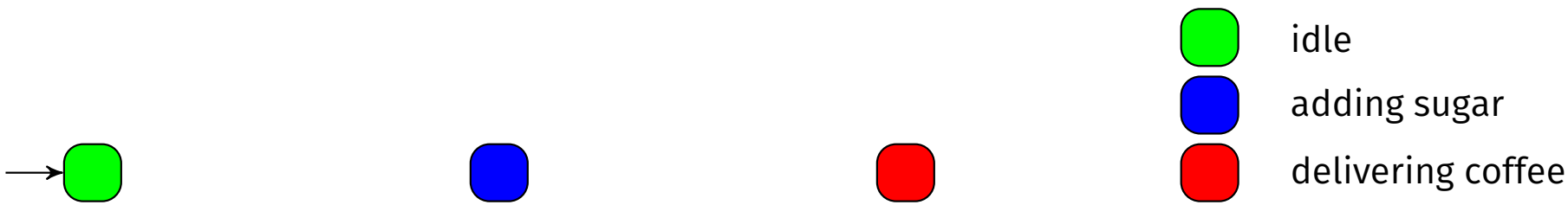
Counterexample

Turing award (2007) to Edmund M. Clarke, Allen Emerson and Joseph Sifakis

Outline

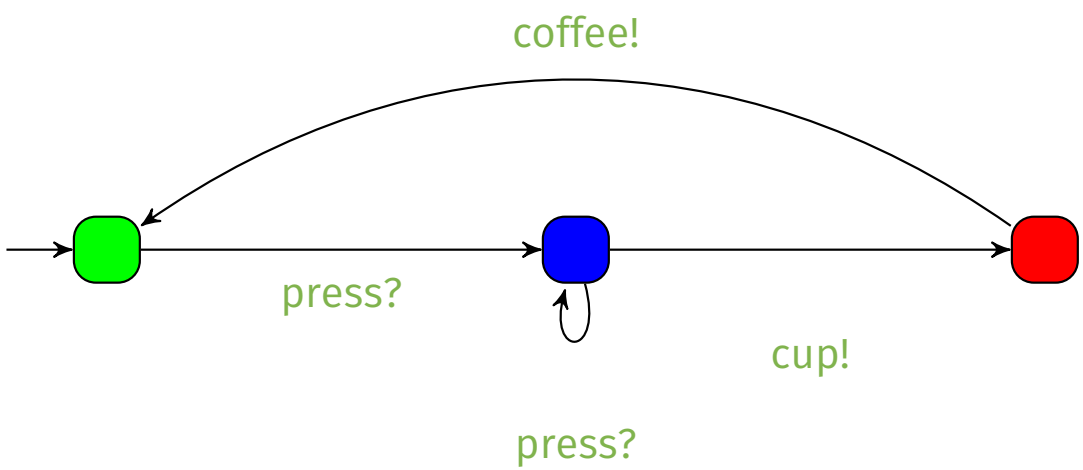
Timed automaton (TA)

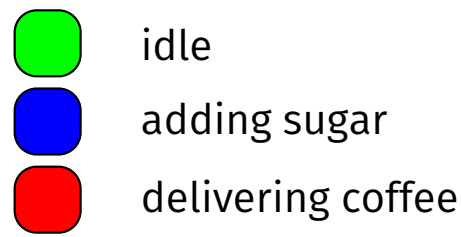
- Finite state automaton (sets of locations)



Timed automaton (TA)

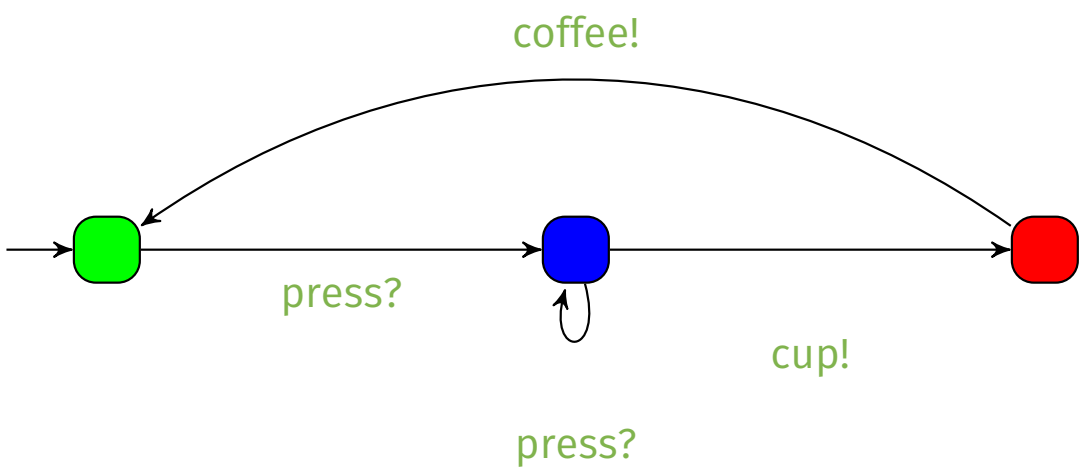
- Finite state automaton (sets of locations and actions)

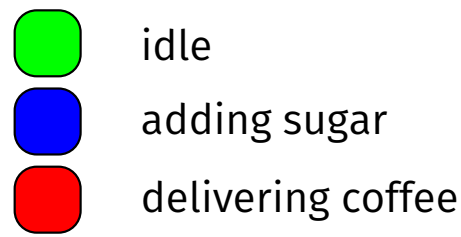




Timed automaton (TA)

- Finite state automaton (sets of locations and actions) augmented with a set X of clocks [Alur and Dill, 1994]
  - Real-valued variables evolving linearly at the same rate





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- Features
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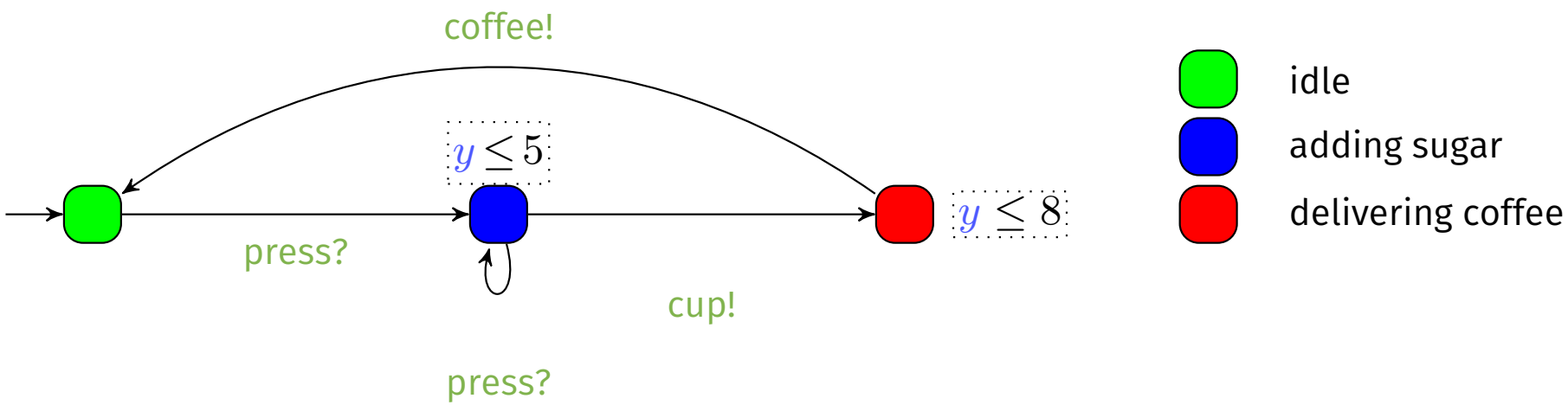

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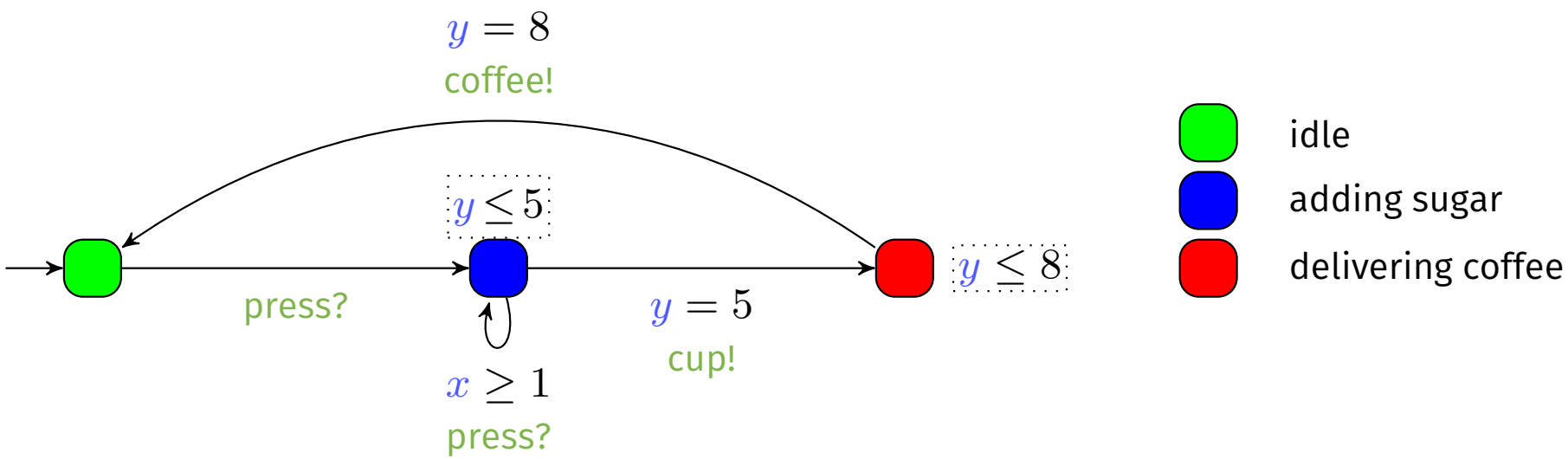
  - Transition guard: property to be verified to enable a transition



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  - Real-valued variables evolving linearly at the same rate
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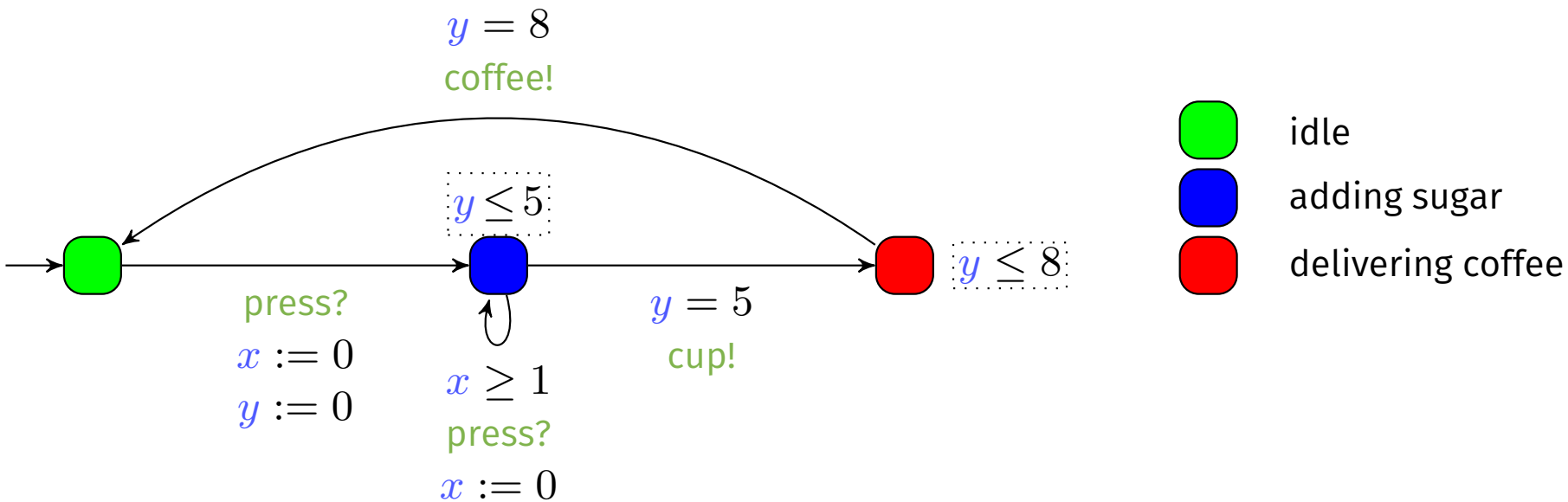
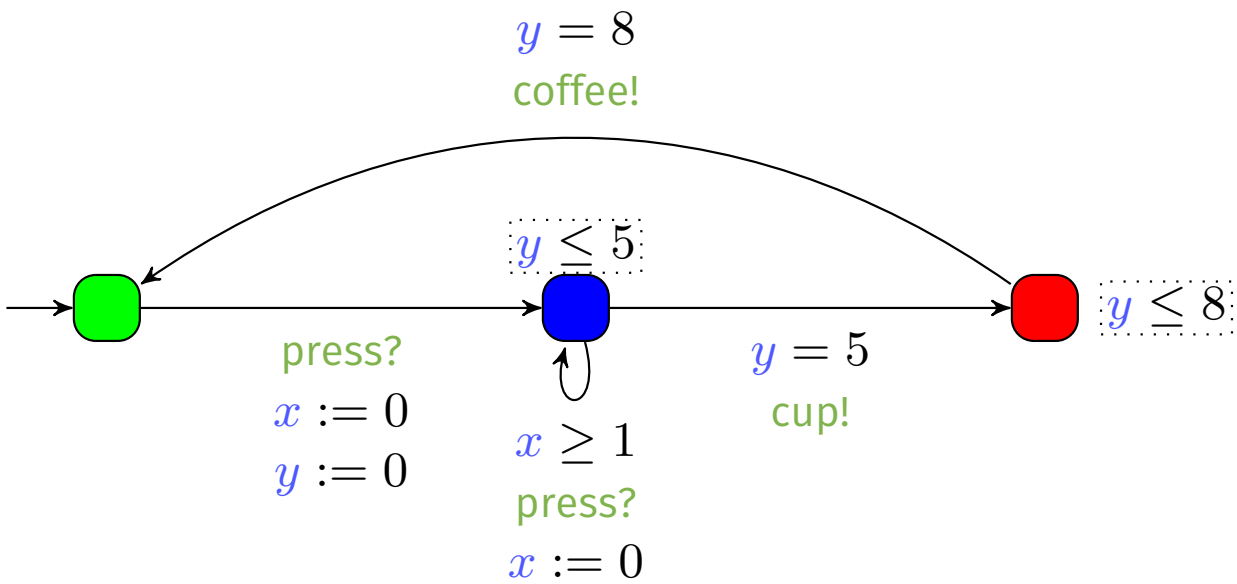
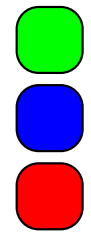
- Features
  - Location invariant: property to be verified to stay at a location
  - Transition guard: property to be verified to enable a transition
  - Clock reset: some of the clocks can be set to 0 along transitions



The most critical system: The coffee machine



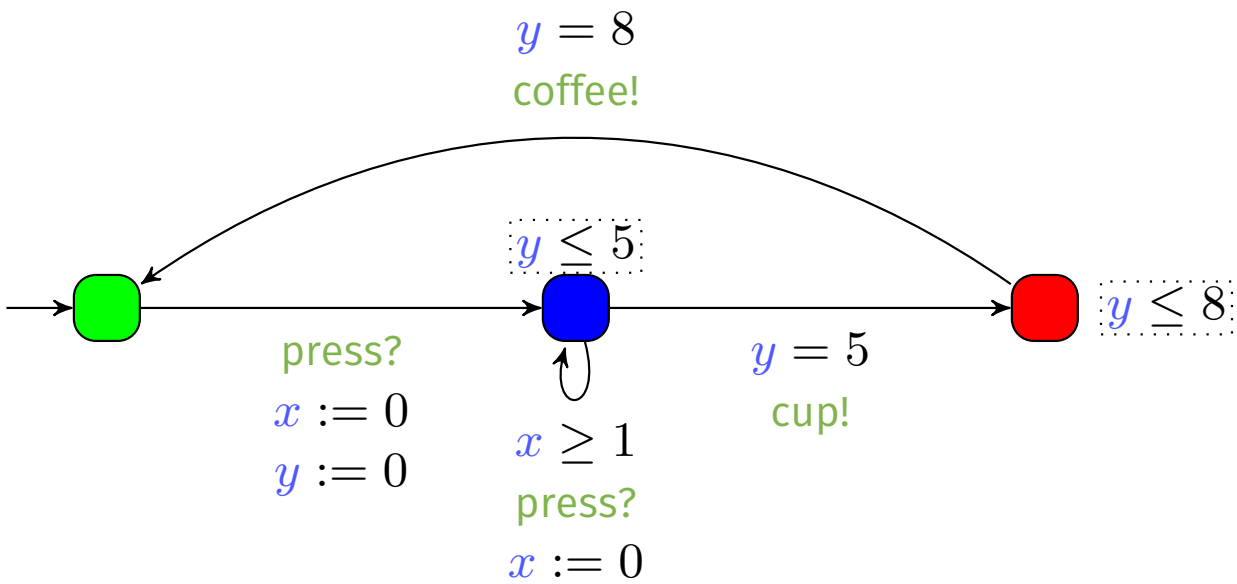


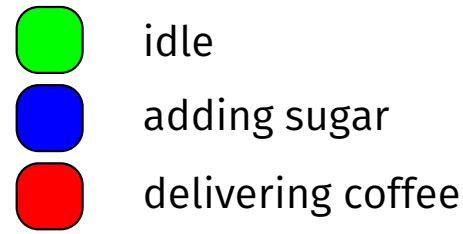
idle

adding sugar

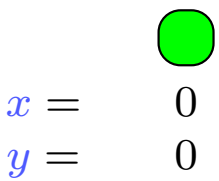
delivering coffee

The most critical system: The coffee machine





- Example of concrete run for the coffee machine
  - Coffee with 2 doses of sugar



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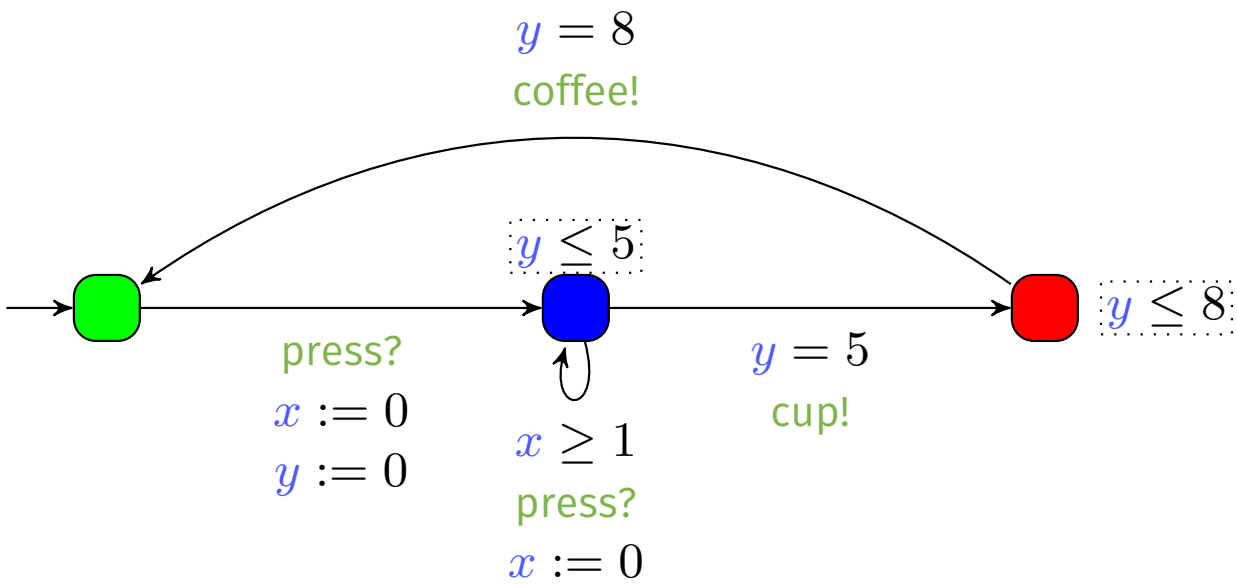

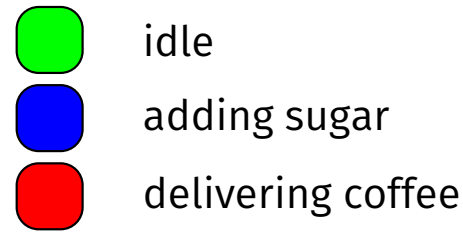

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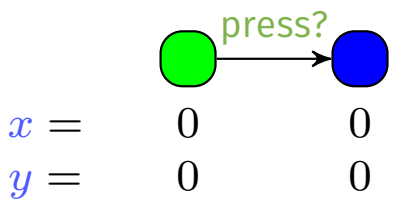

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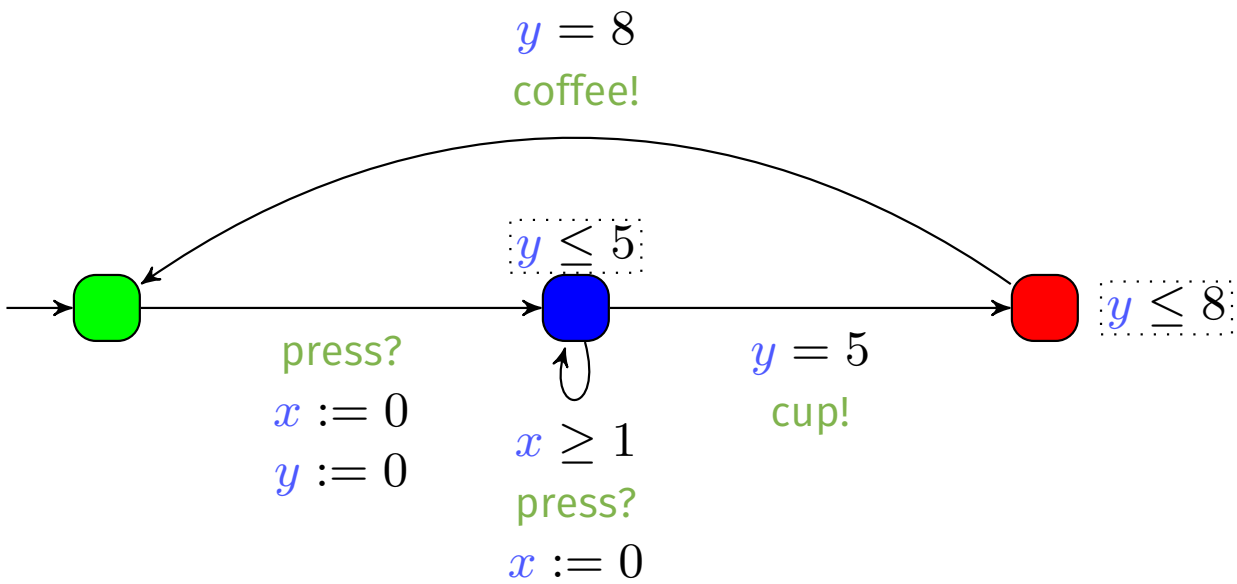

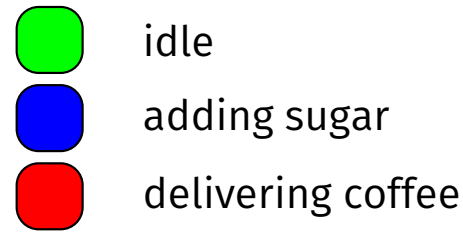

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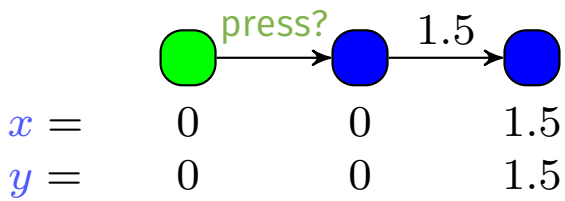

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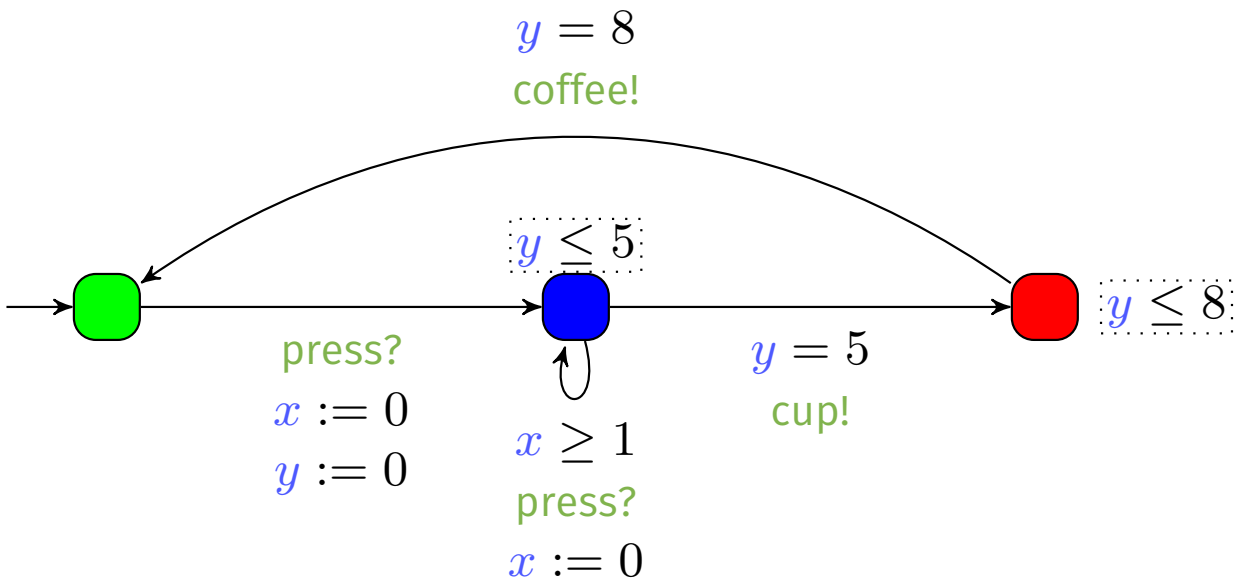

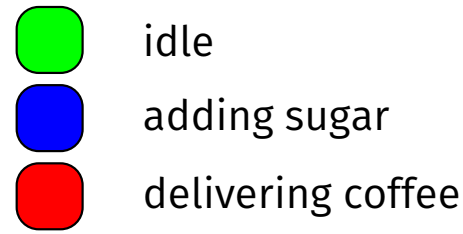

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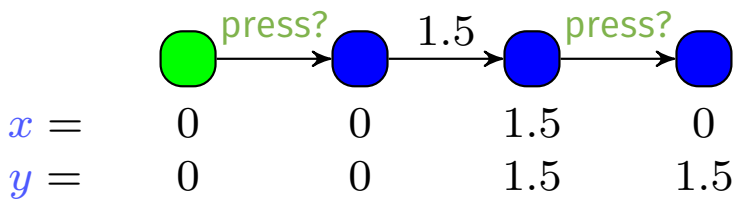

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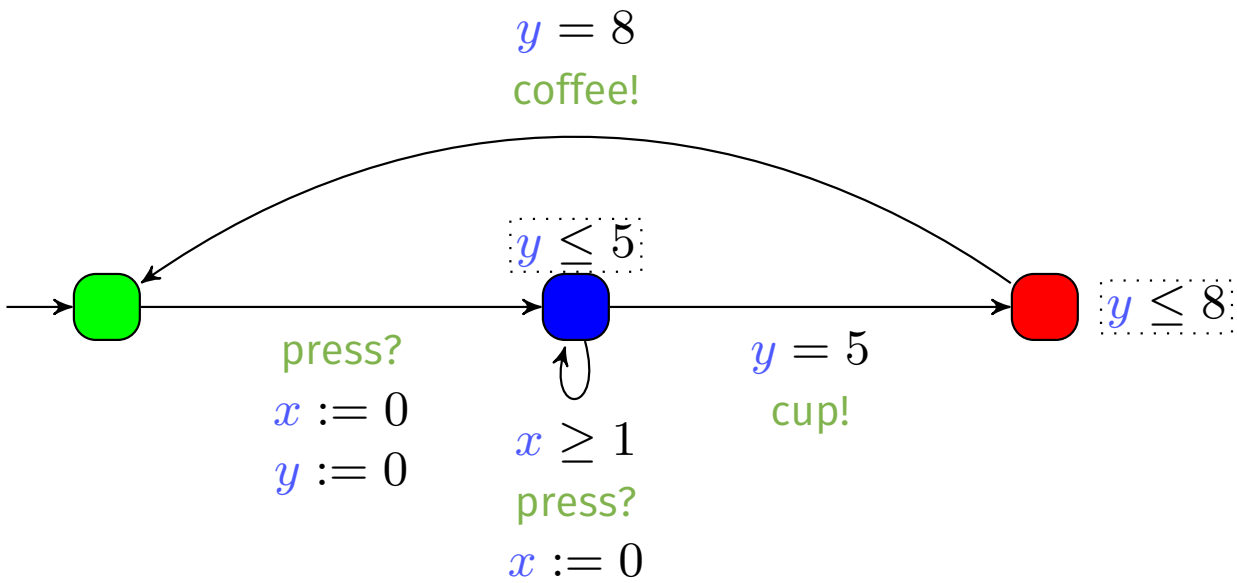

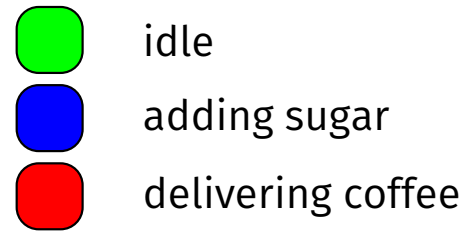

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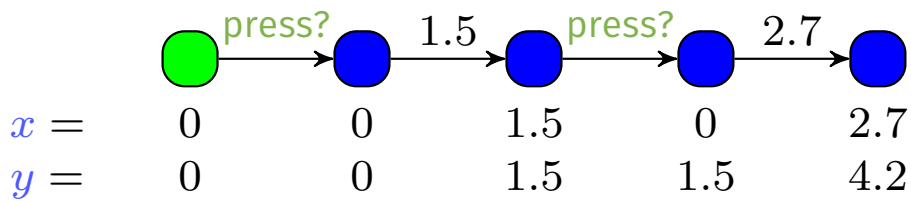

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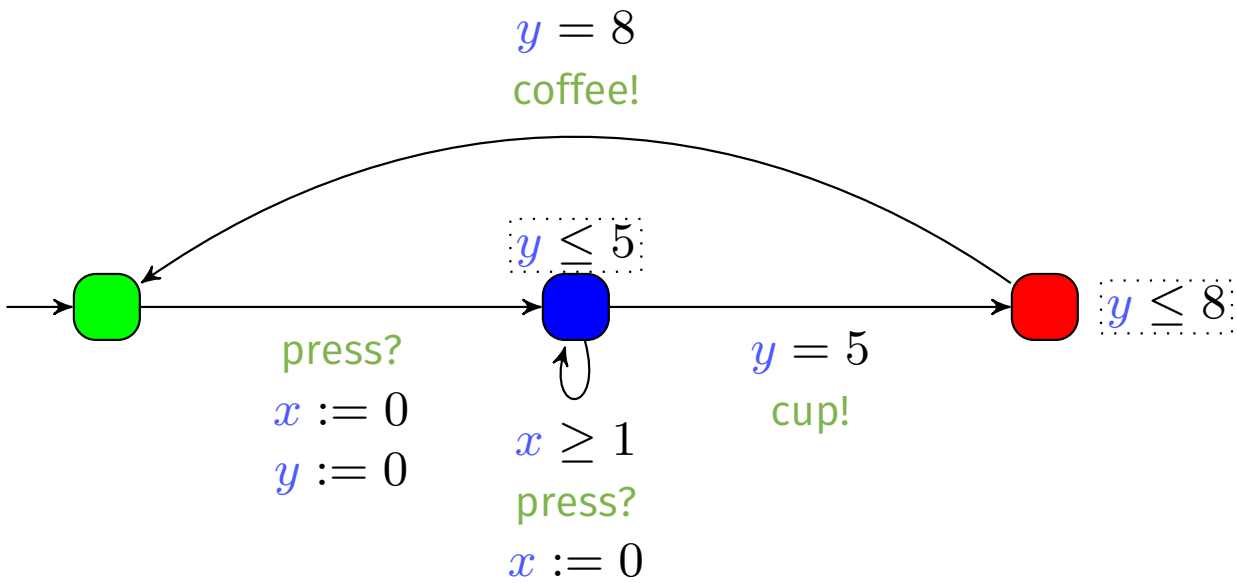

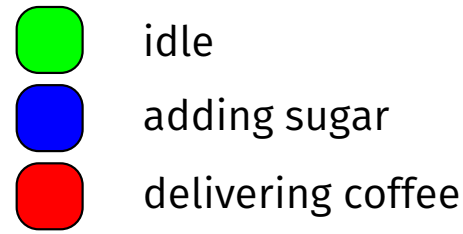

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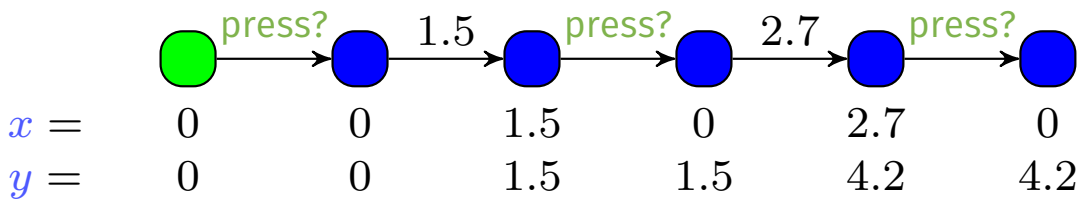

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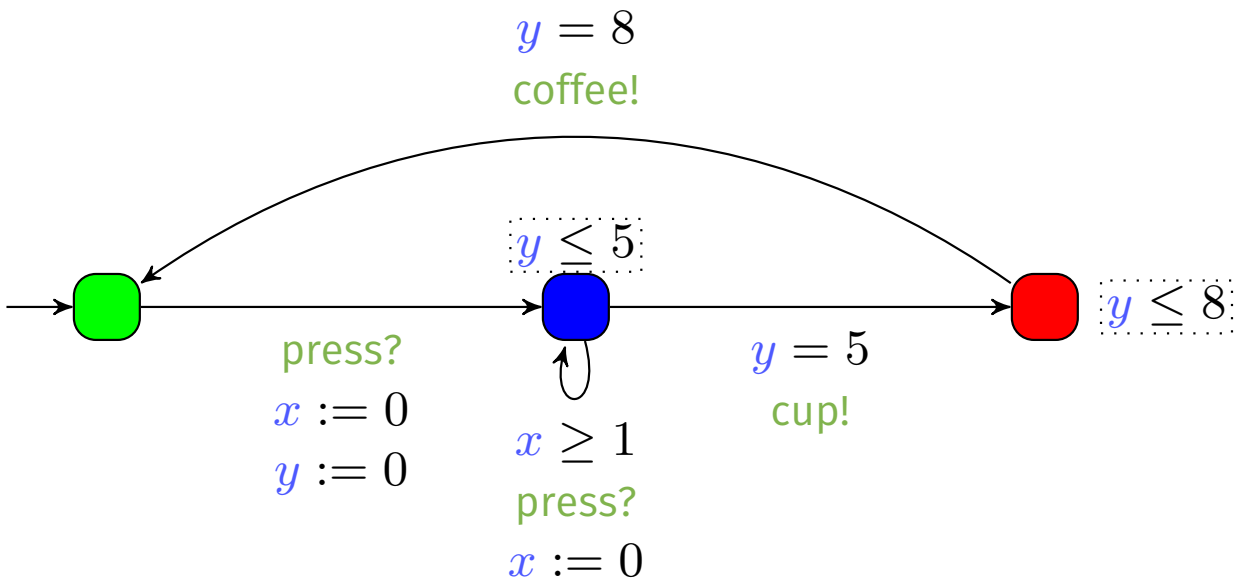

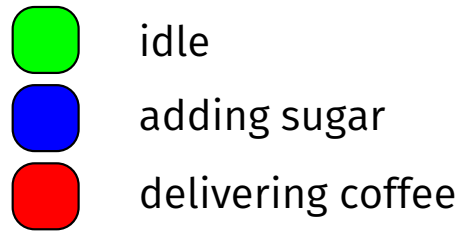

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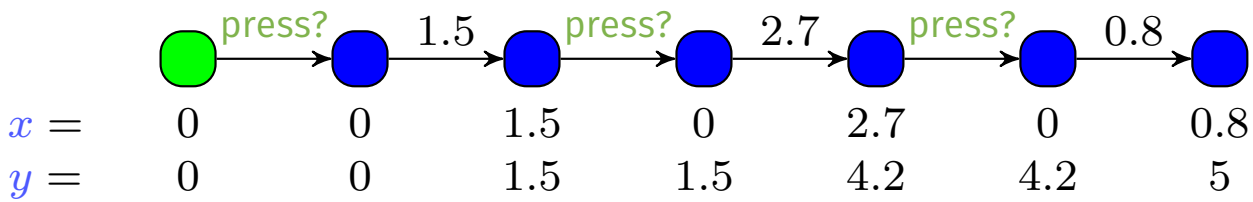

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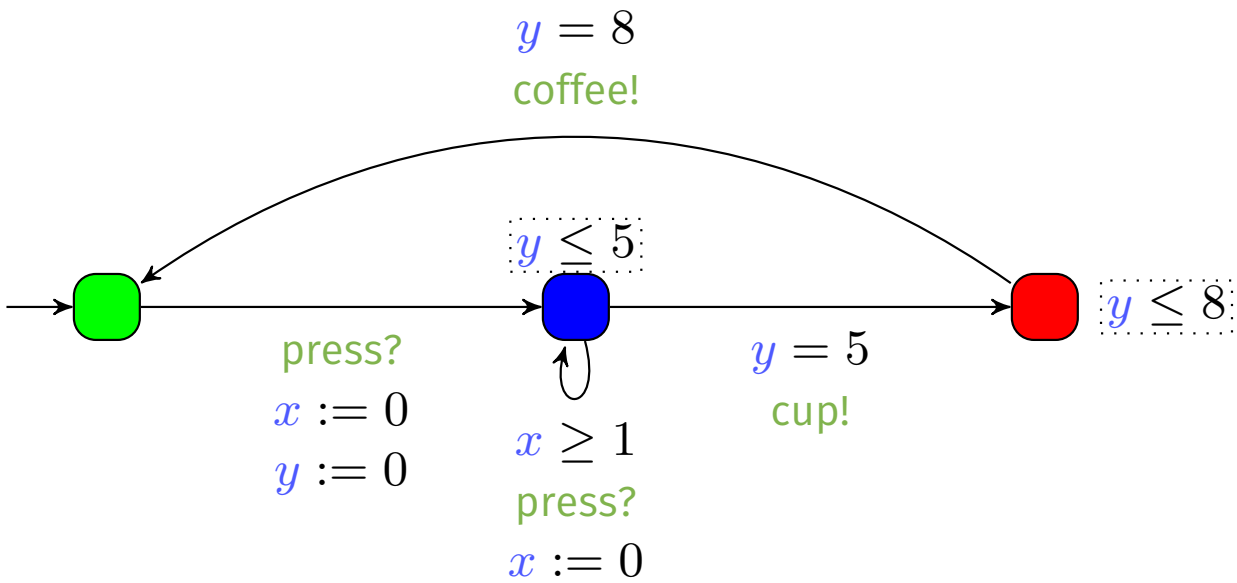

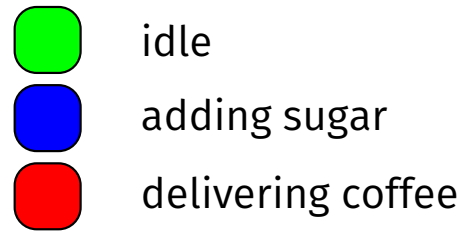

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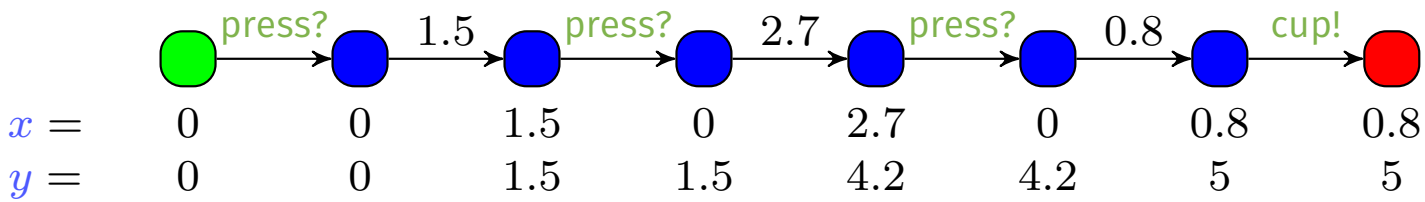

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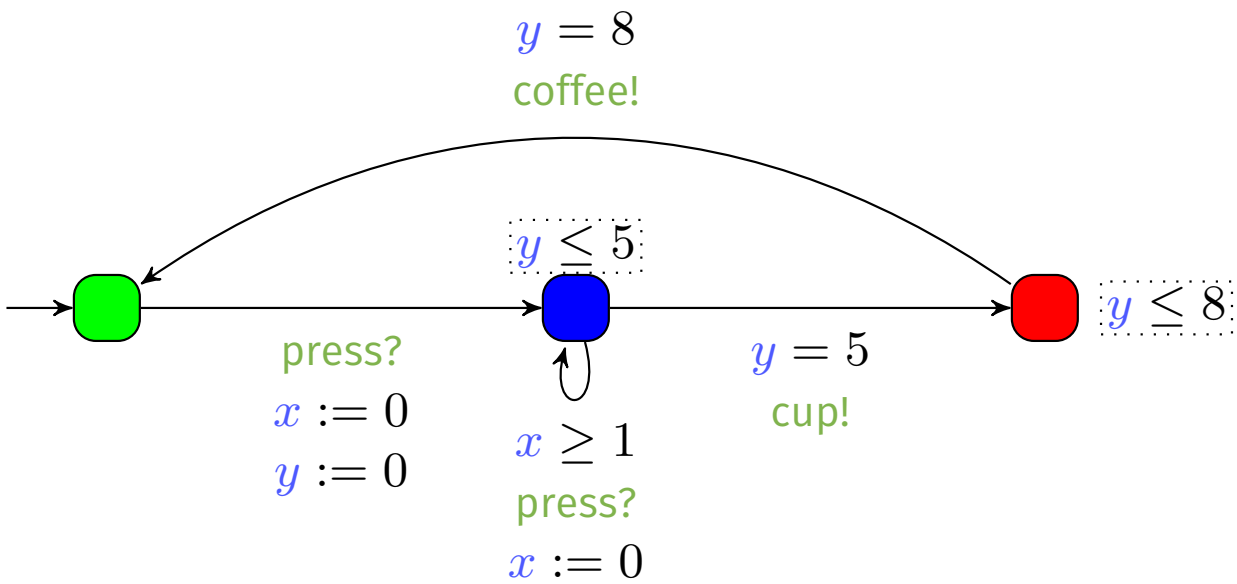

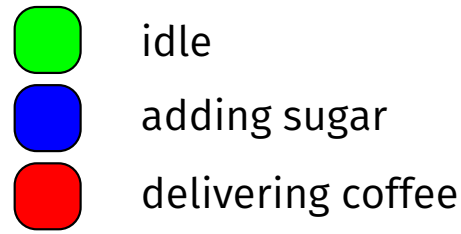

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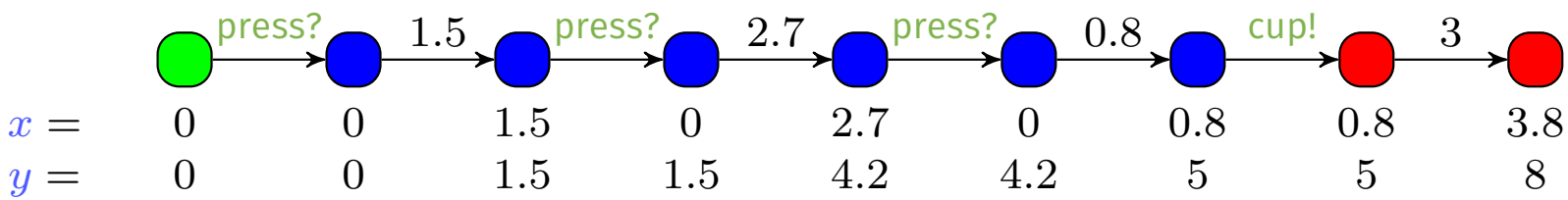

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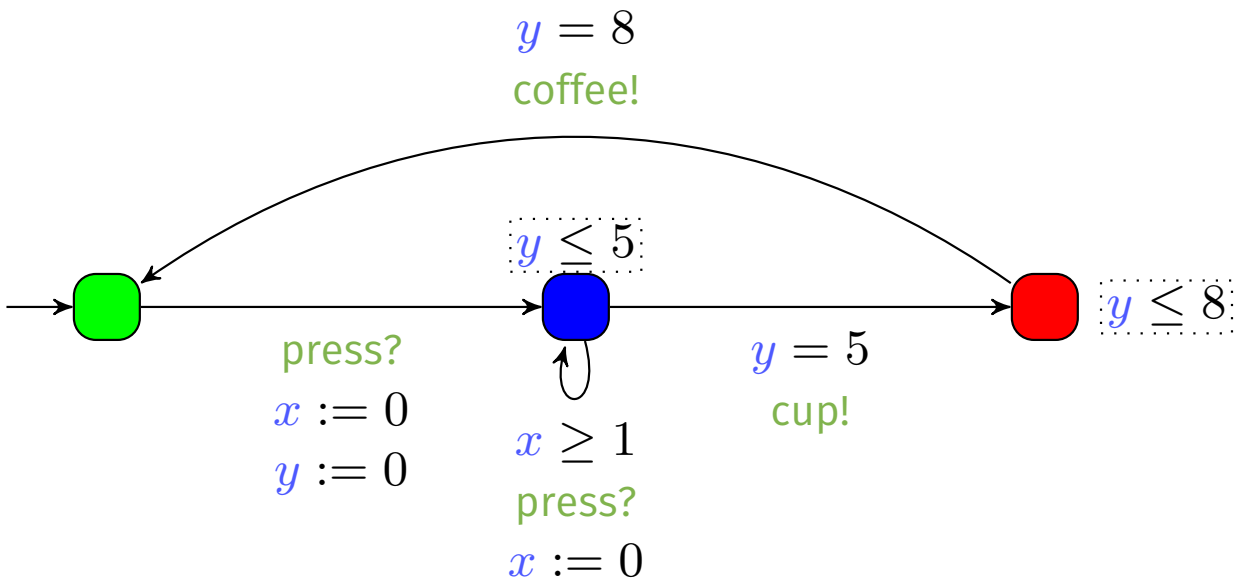

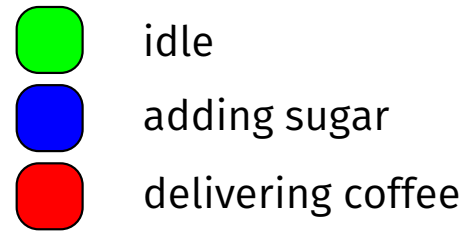

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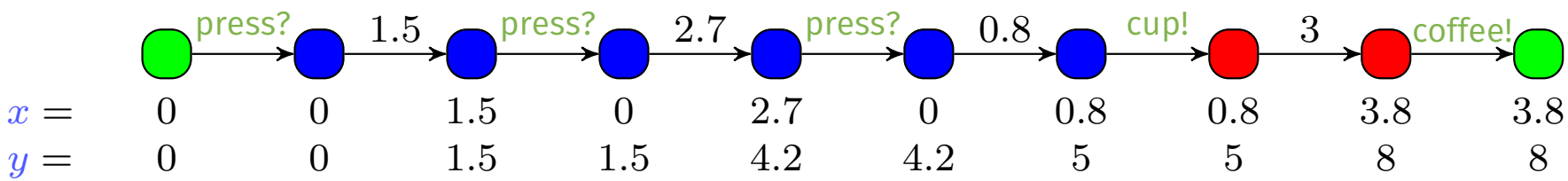


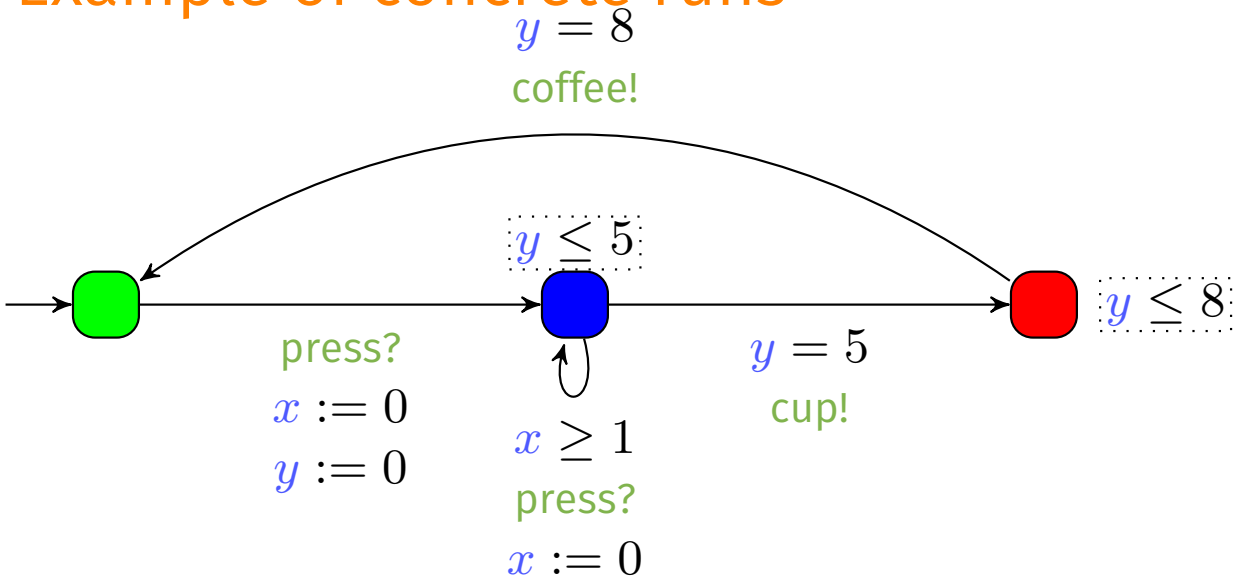
Concrete semantics of timed automata

- Concrete state of a TA: pair (l, w), where
  - l is a location,
  - w is a valuation of each clock

  Example: $\left(\right.$  $, \begin{pmatrix} x=1.2 \\ y=3.7 \end{pmatrix}\left.\right)$

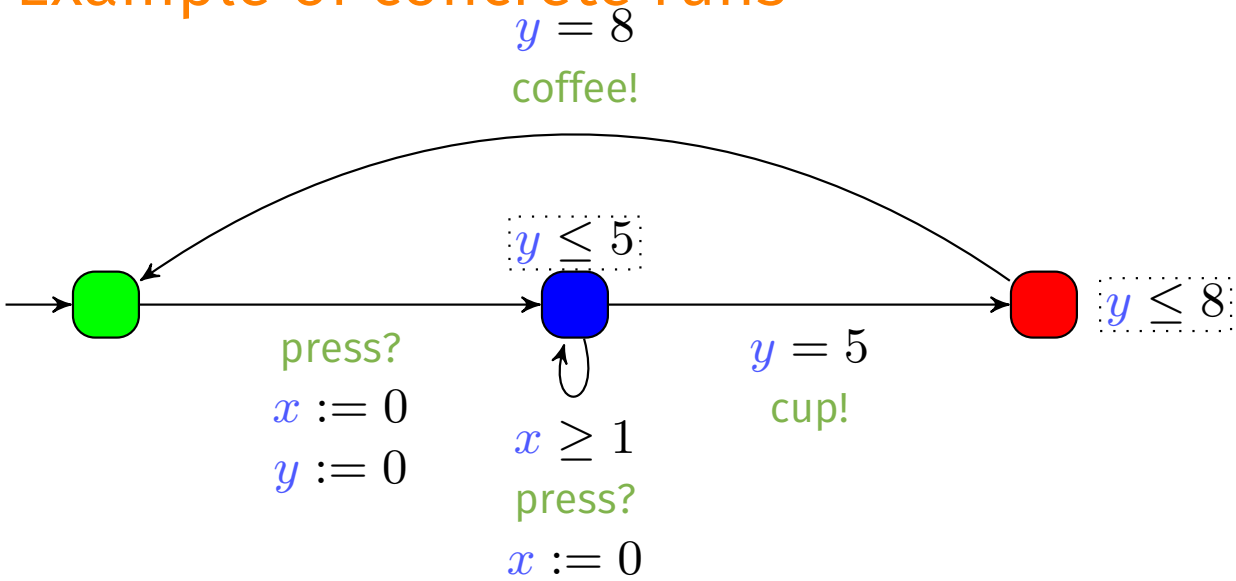
- Concrete run: alternating sequence of concrete states and actions or time elapse

Example of concrete runs

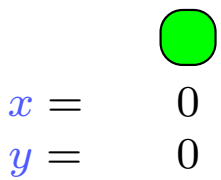


- Possible concrete runs for the coffee machine

Example of concrete runs



- Possible concrete runs for the coffee machine
  - Coffee with no sugar



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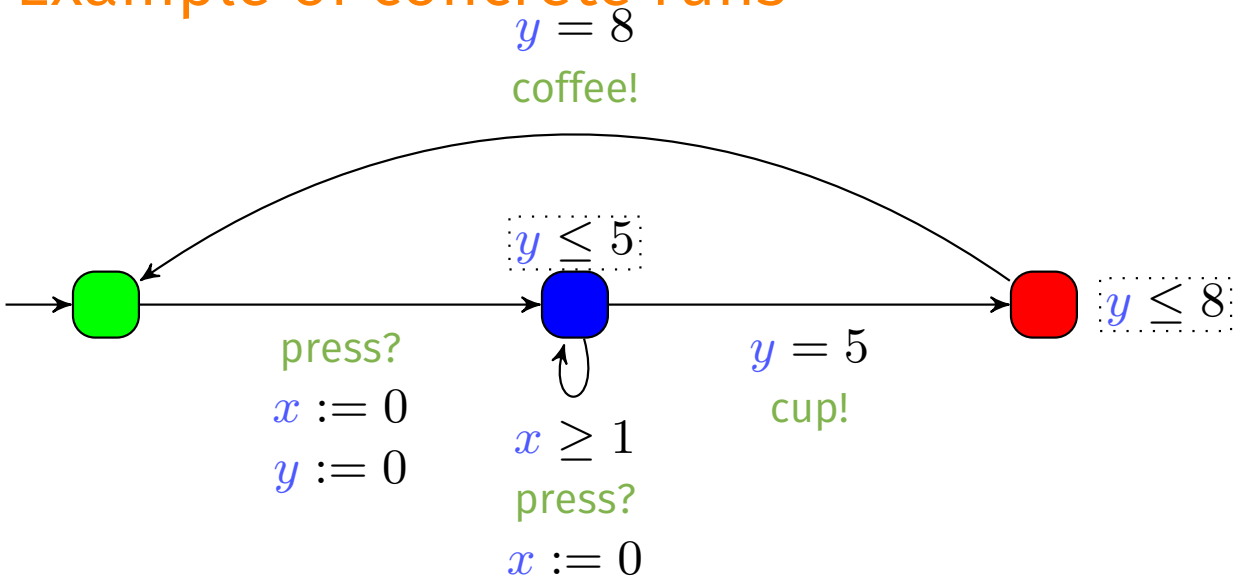

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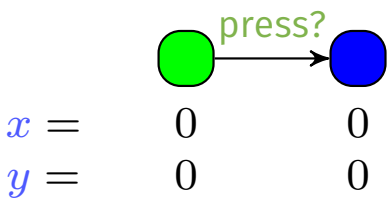

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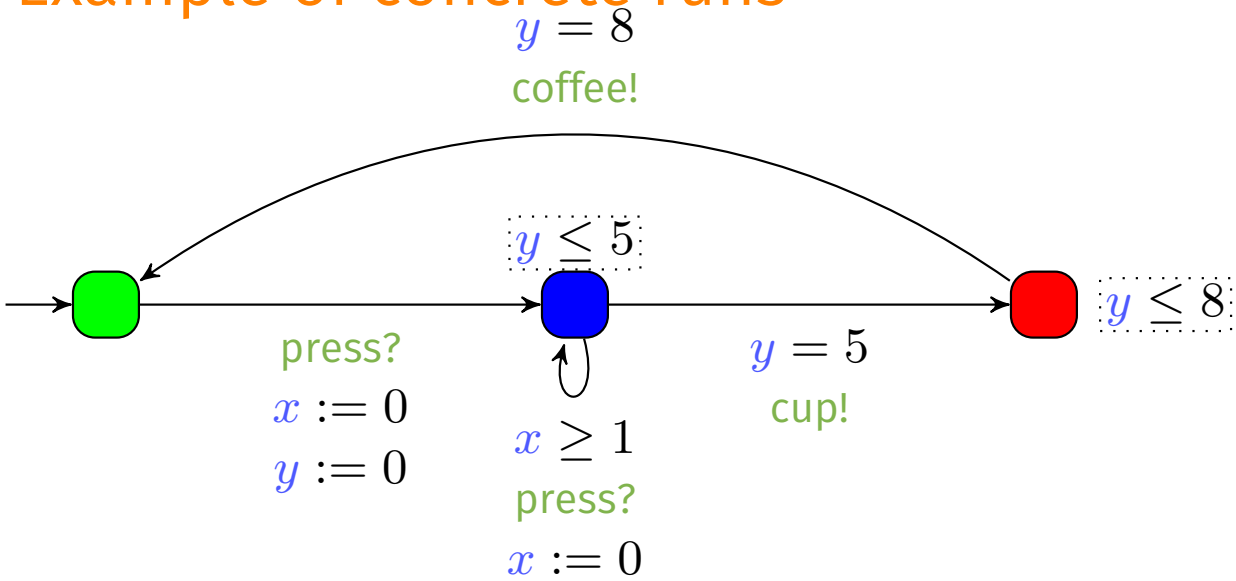

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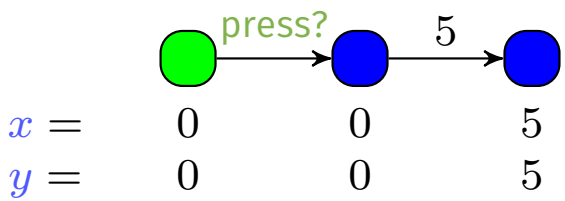
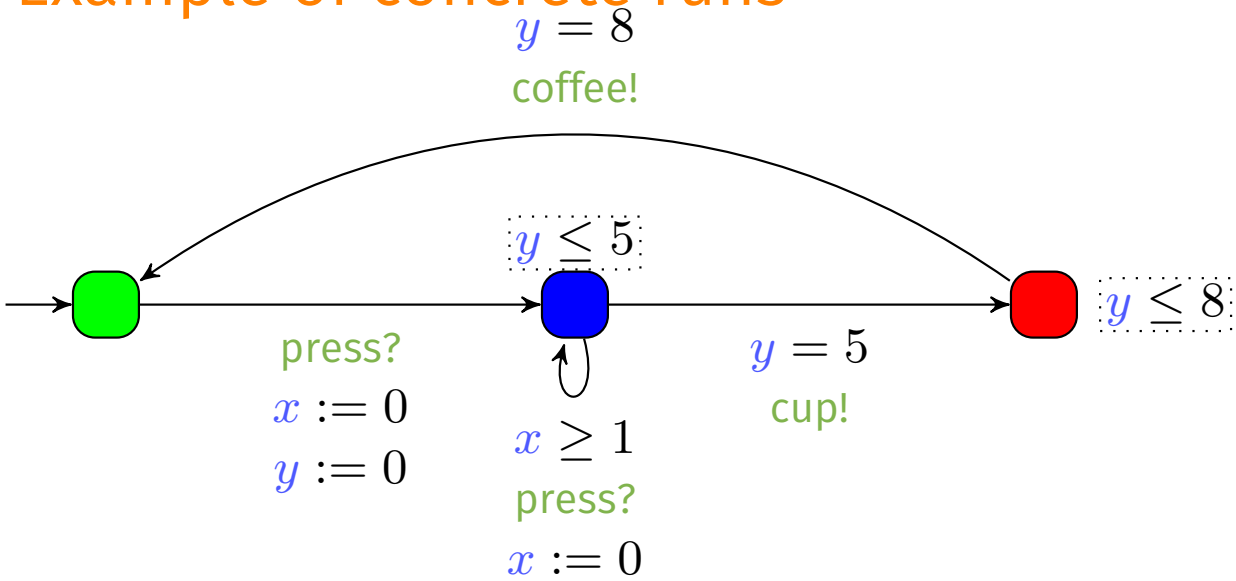
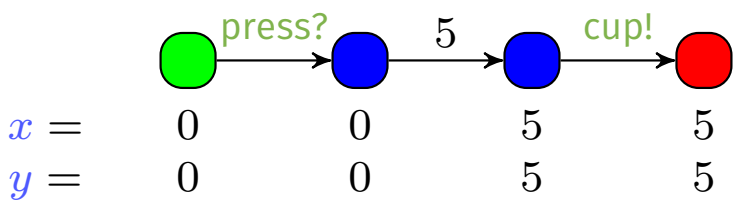


Example of concrete runs



- Possible concrete runs for the coffee machine
  - Coffee with no sugar



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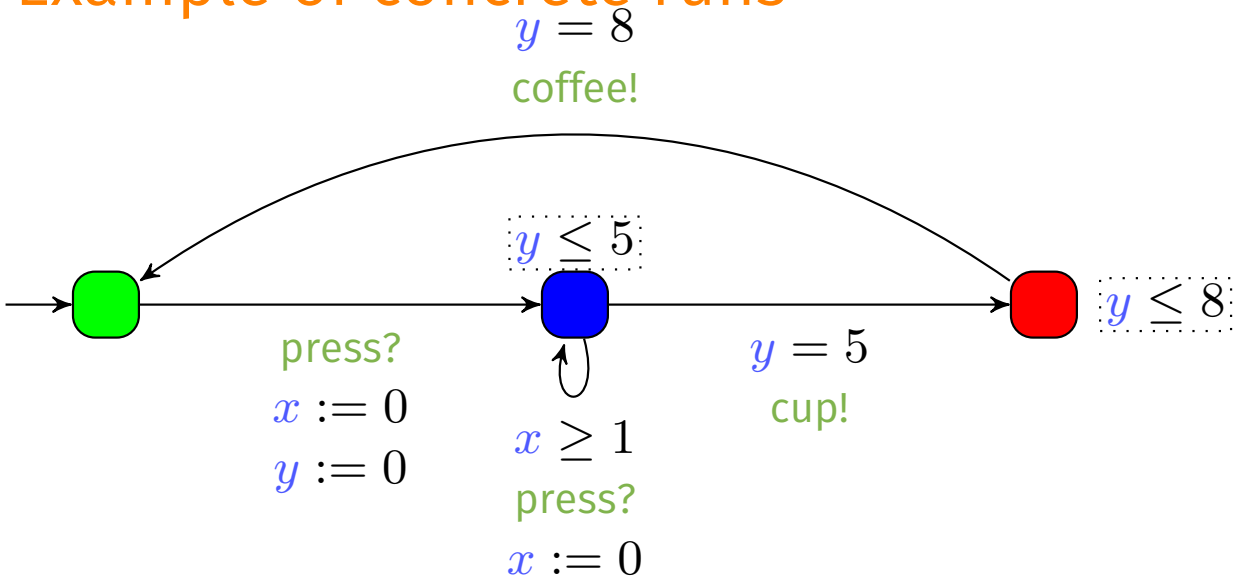

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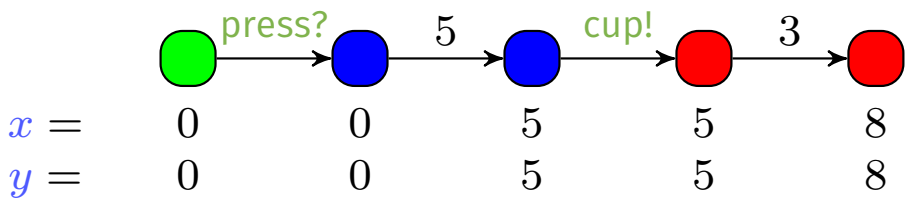

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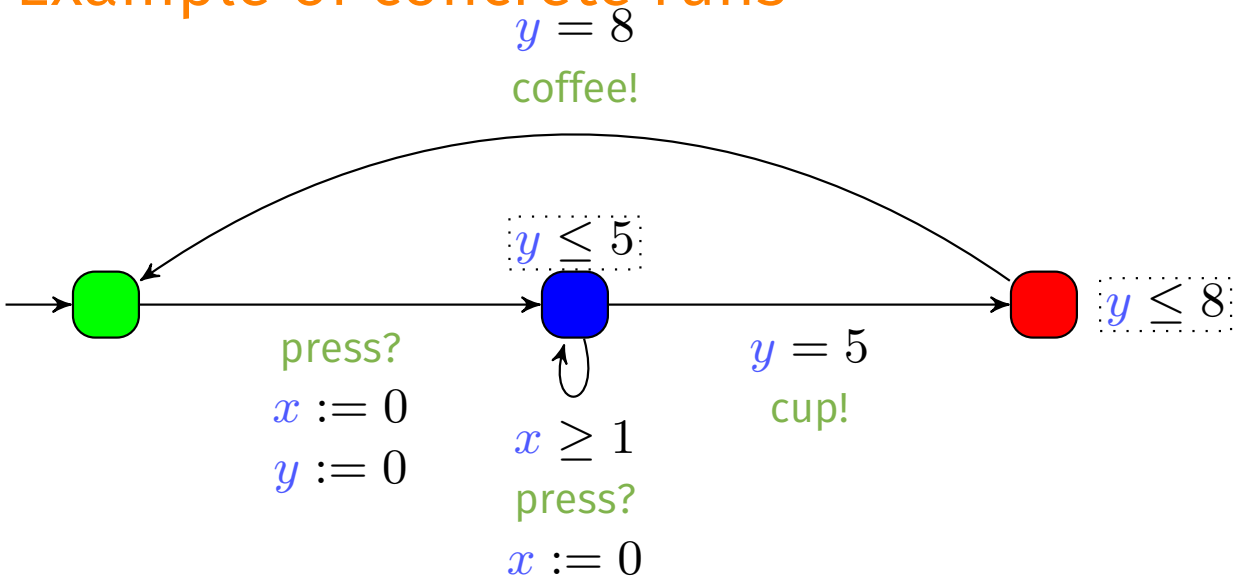

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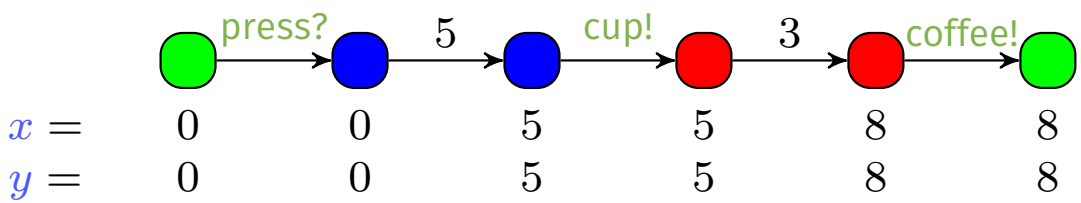

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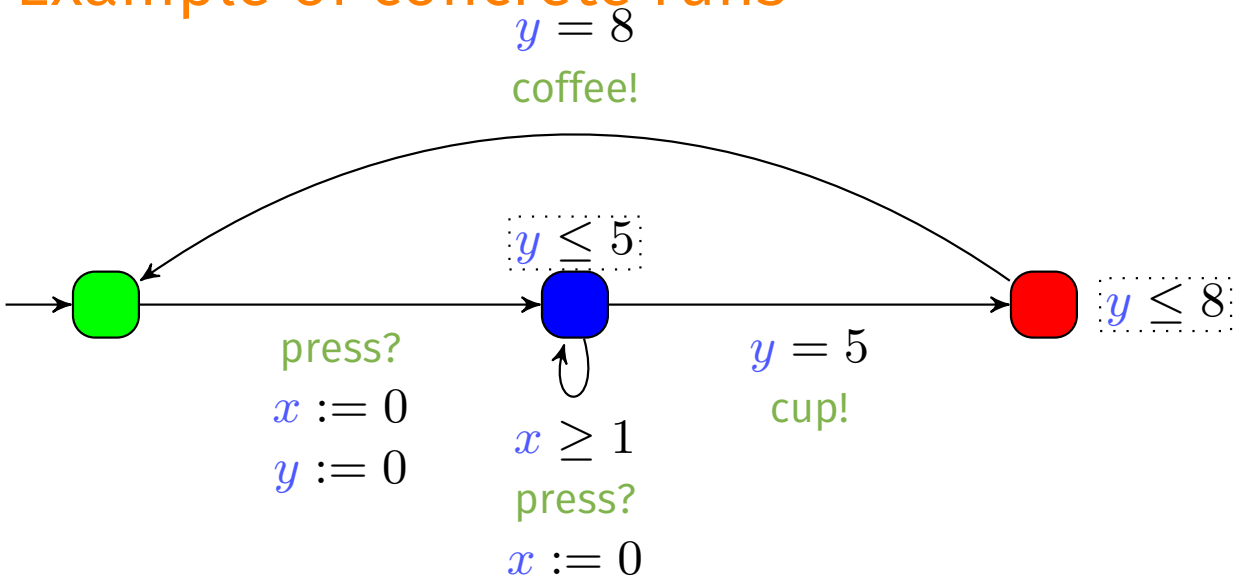

- Possible concrete runs for the coffee machine
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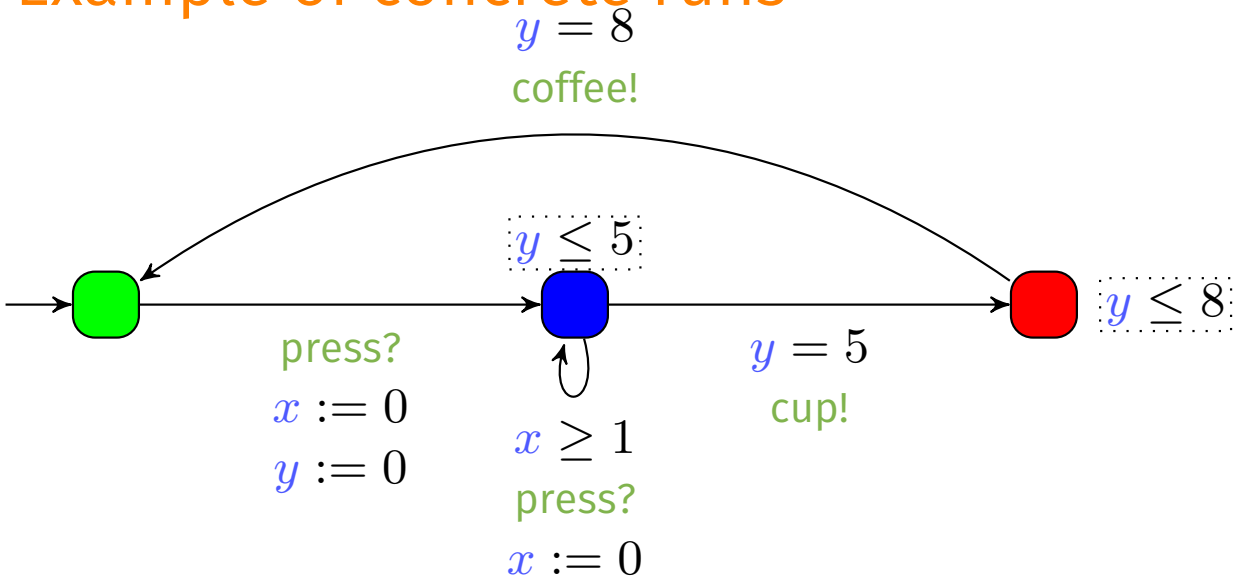
$x =$	0	0	5	5	8	8
$y =$	0	0	5	5	8	8

  - Coffee with 2 doses of sugar

$x =$	0
$y =$	0

Example of concrete runs



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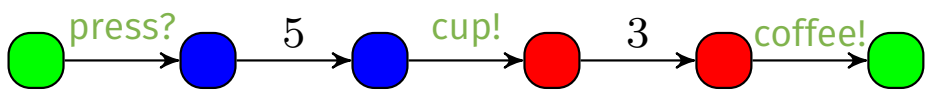
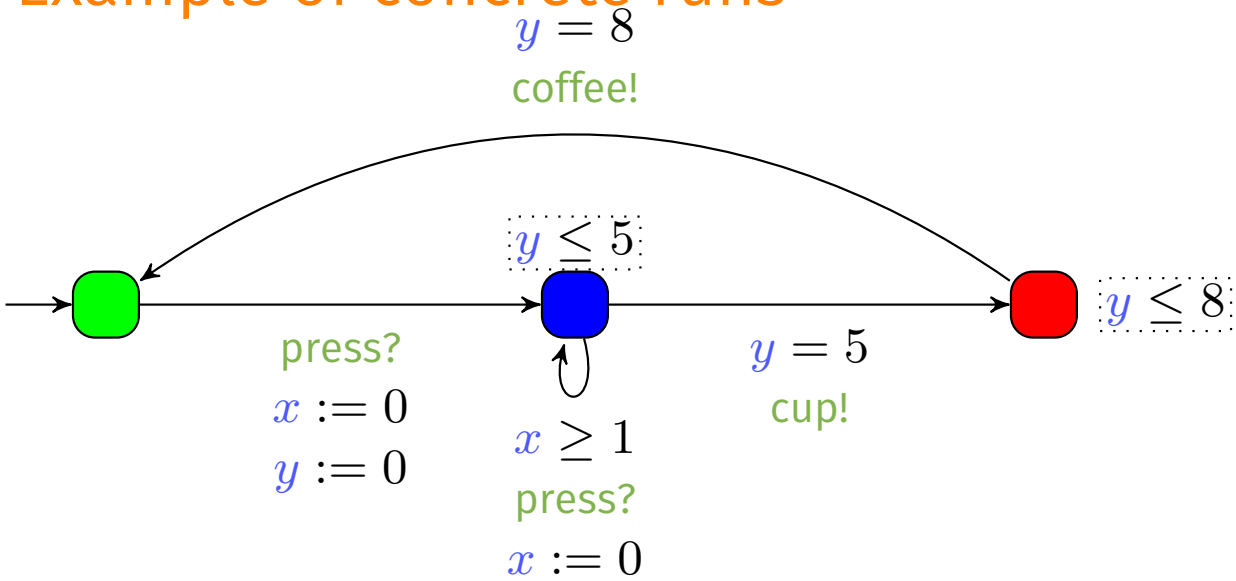


$x =$	0	0	5	5	8	8
$y =$	0	0	5	5	8	8

  - Coffee with 2 doses of sugar

$x =$	0	0
$y =$	0	0

Example of concrete runs



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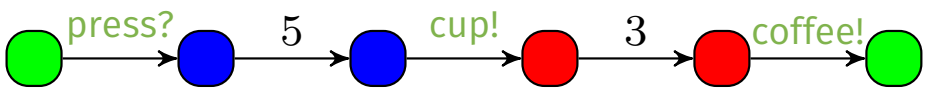
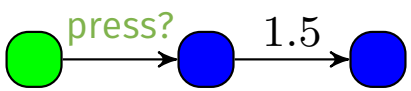


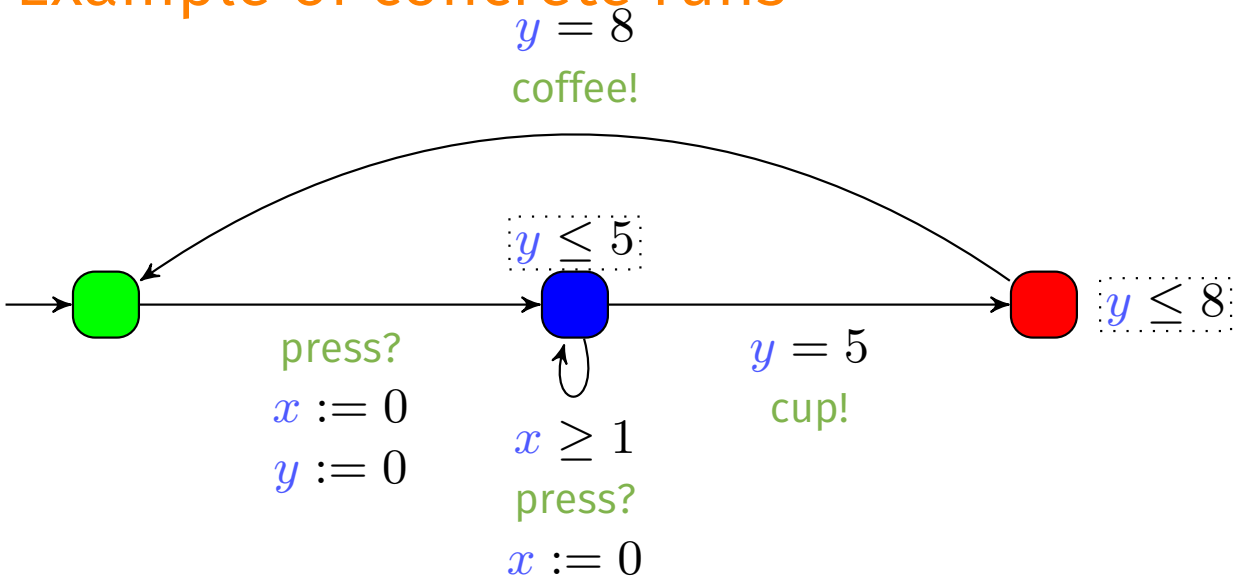
$x =$	0	0	5	5	8	8
$y =$	0	0	5	5	8	8

  - Coffee with 2 doses of sugar



$x =$	0	0	1.5
$y =$	0	0	1.5

Example of concrete runs



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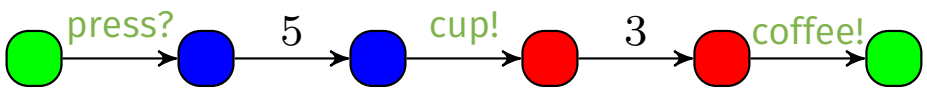
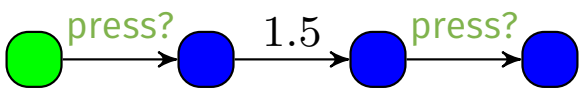


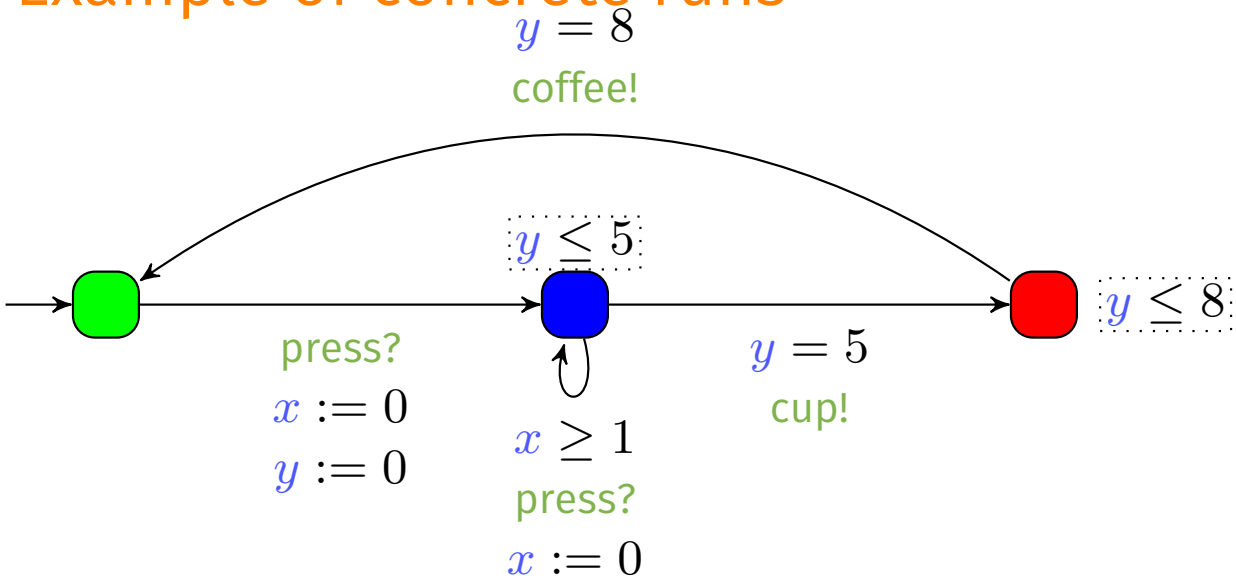
$x =$	0	0	5	5	8	8
$y =$	0	0	5	5	8	8

  - Coffee with 2 doses of sugar



$x =$	0	0	1.5	0
$y =$	0	0	1.5	1.5

Example of concrete runs



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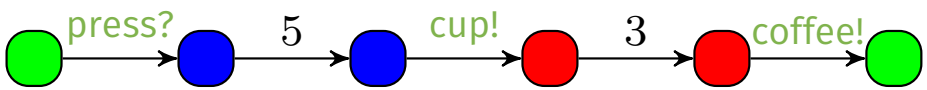
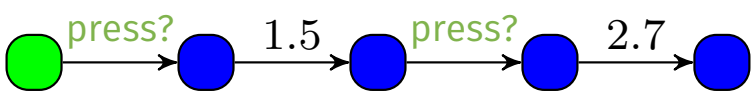


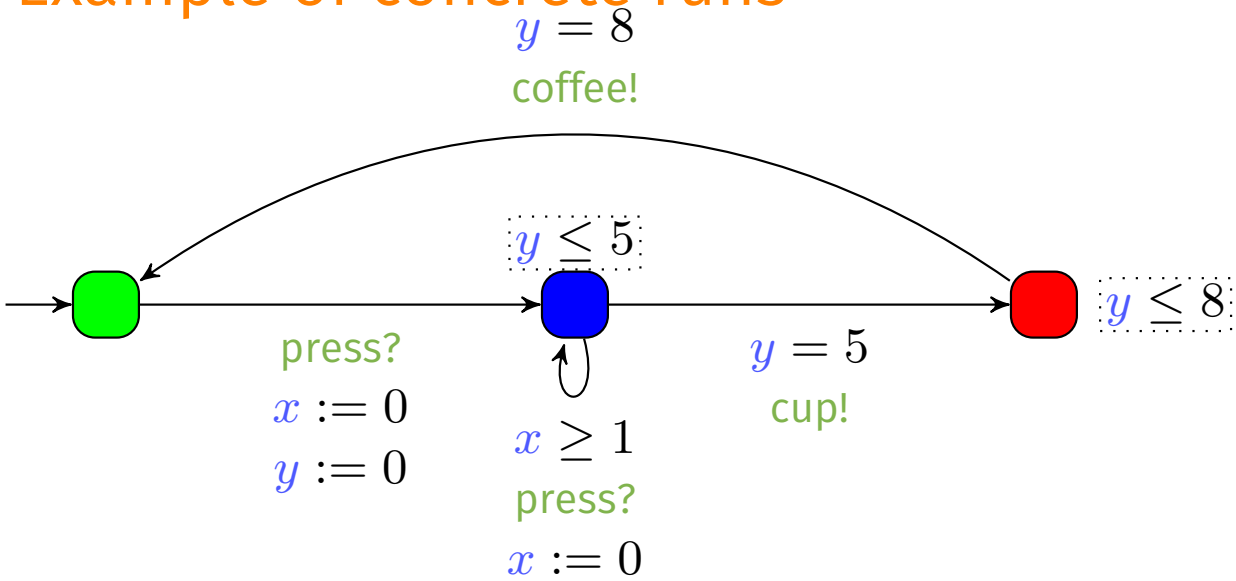
$x =$	0	0	5	5	8	8
$y =$	0	0	5	5	8	8

  - Coffee with 2 doses of sugar



$x =$	0	0	1.5	0	2.7
$y =$	0	0	1.5	1.5	4.2

Example of concrete runs



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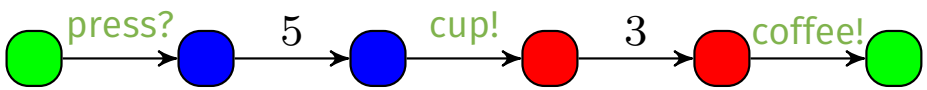
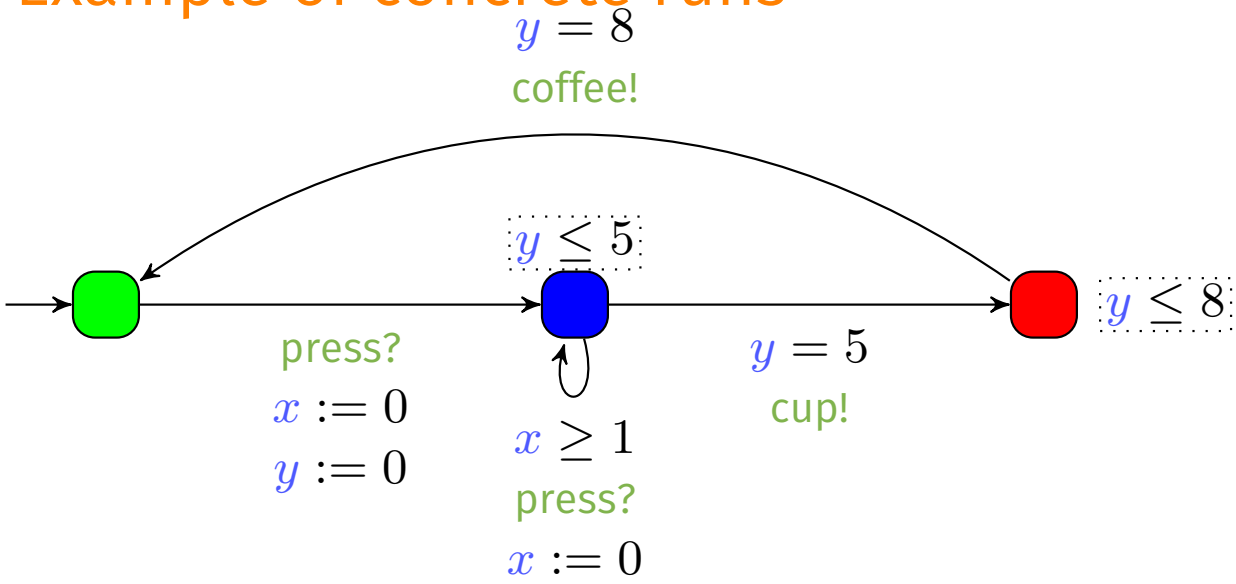


$x =$	0	0	5	5	8	8
$y =$	0	0	5	5	8	8

  - Coffee with 2 doses of sugar

$x =$	0	0	1.5	0	2.7	0
$y =$	0	0	1.5	1.5	4.2	4.2

Example of concrete runs



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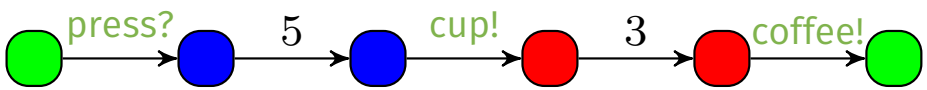
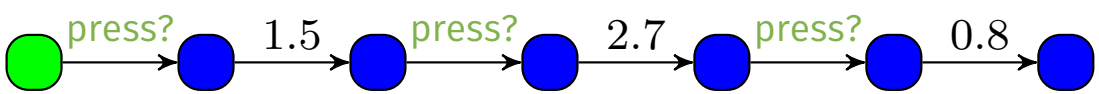


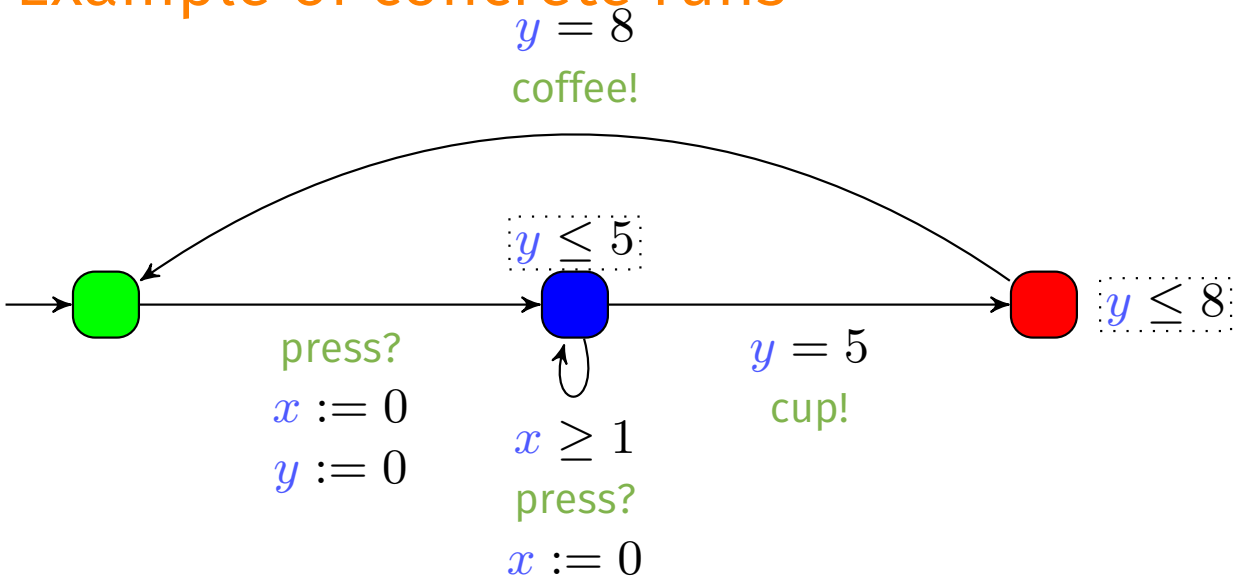
$x =$	0	0	5	5	8	8
$y =$	0	0	5	5	8	8

  - Coffee with 2 doses of sugar



$x =$	0	0	1.5	0	2.7	0	0.8
$y =$	0	0	1.5	1.5	4.2	4.2	5

Example of concrete runs



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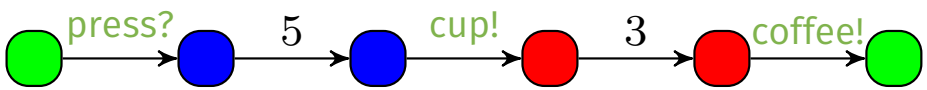
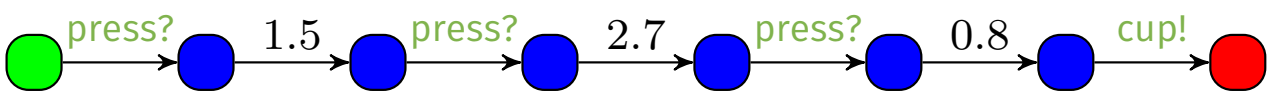


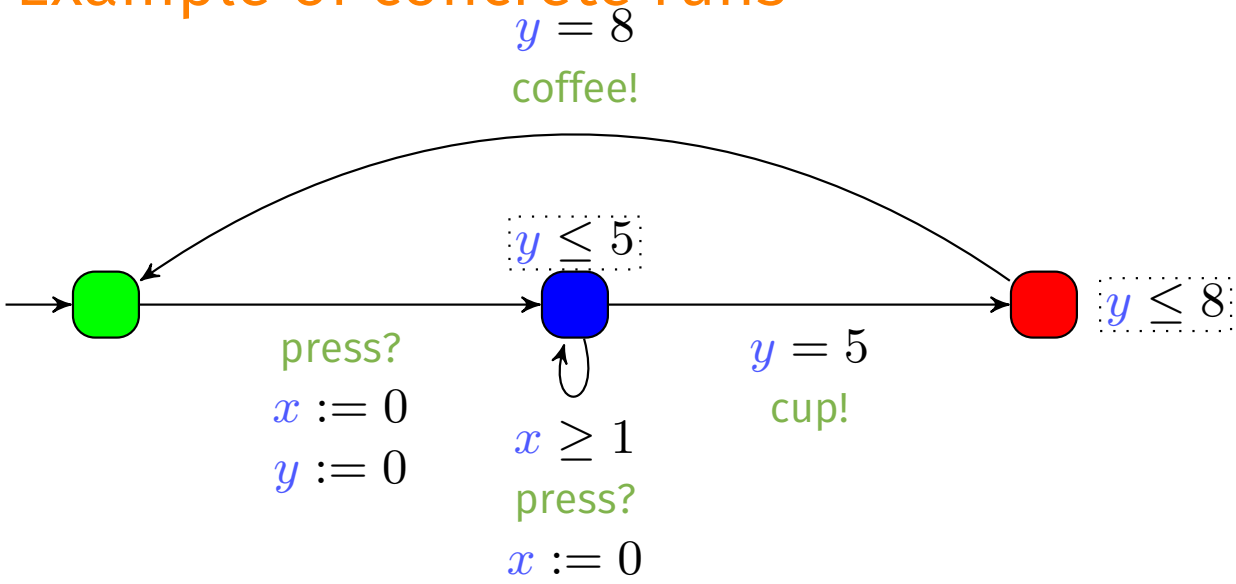
$x =$	0	0	5	5	8	8
$y =$	0	0	5	5	8	8

  - Coffee with 2 doses of sugar



$x =$	0	0	1.5	0	2.7	0	0.8	0.8
$y =$	0	0	1.5	1.5	4.2	4.2	5	5

Example of concrete runs



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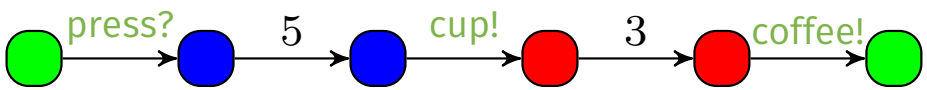

$x =$	0	0	5	5	8	8
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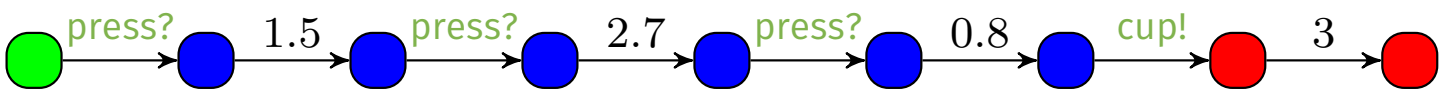
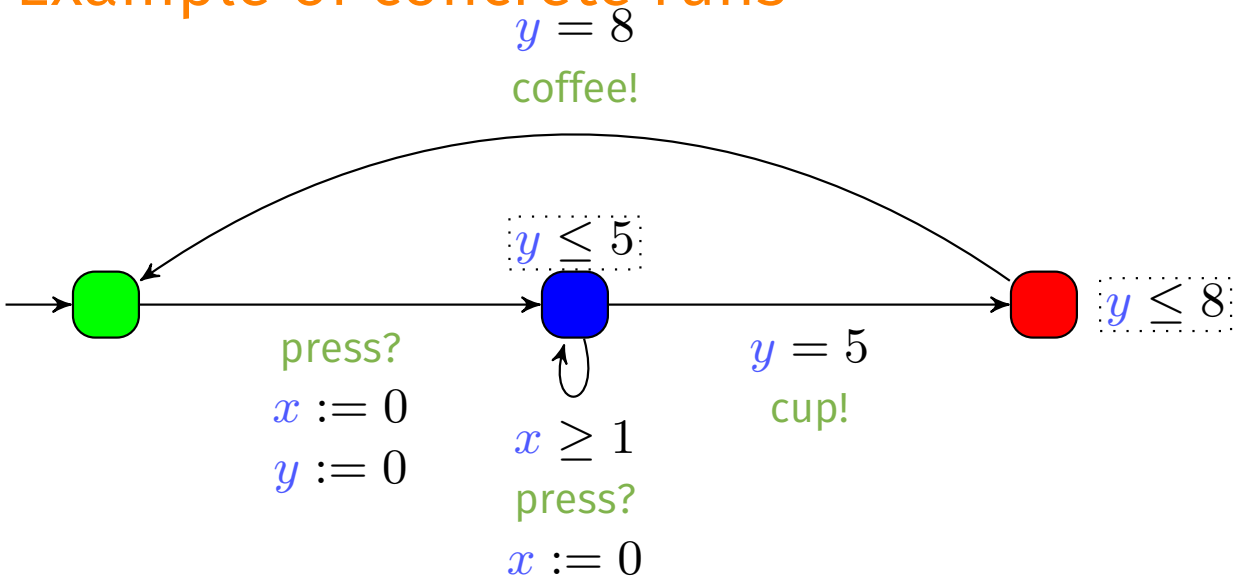


$x =$	0	0	1.5	0	2.7	0	0.8	0.8	3.8
$y =$	0	0	1.5	1.5	4.2	4.2	5	5	8

Example of concrete runs



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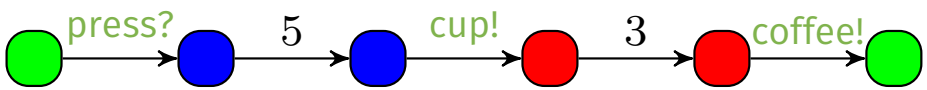

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$y =$	0	0	5	5	8	8

  - Coffee with 2 doses of sugar

$x =$	0	0	1.5	0	2.7	0	0.8	0.8	3.8	3.8
$y =$	0	0	1.5	1.5	4.2	4.2	5	5	8	8

Timed automata: A success story

- An expressive formalism
  - Dense time
  - Concurrency
- A tractable verification in theory
  - Reachability is PSPACE-complete [Alur and Dill, 1994]
- A very efficient verification in practice
  - Symbolic verification: relatively insensitive to constants
  - Several model checkers, notably UPPAAL [Larsen et al., 1997]
  - Long list of successful case studies

Outline

Beyond timed model checking: parameter synthesis

- Verification for one set of constants does not usually guarantee the correctness for other values

- Challenges
  - Numerous verifications: is the system correct for any value within $[40; 60]$?
  - Optimization: until what value can we increase 10?
  - Robustness [Markey, 2011]: What happens if 50 is implemented with 49.99?
  - System incompletely specified: Can I verify my system even if I don't know the period value with full certainty?

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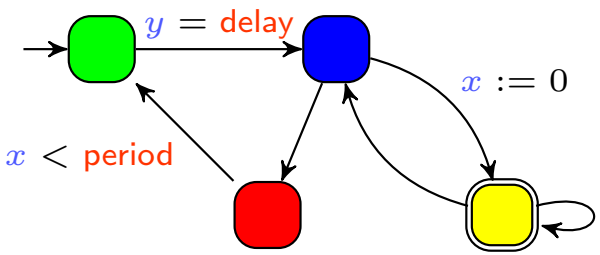
- Parameter synthesis
  - Consider that timing constants are unknown constants (parameters)

timed model checking



A model of the system

$?$

$\models$

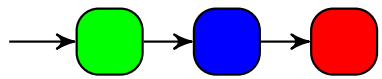
is unreachable

A property to be satisfied

- Question: does the model of the system satisfy the property?

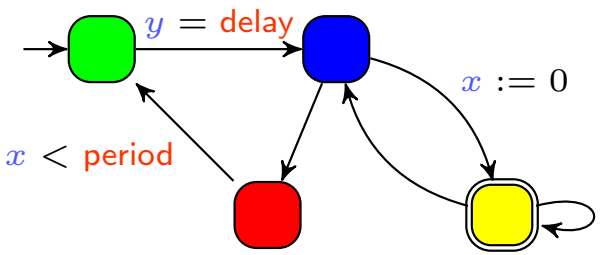
Yes

No



Counterexample

Parametric timed model checking



A model of the system

$?$

$\models$

A property to be satisfied

is unreachable

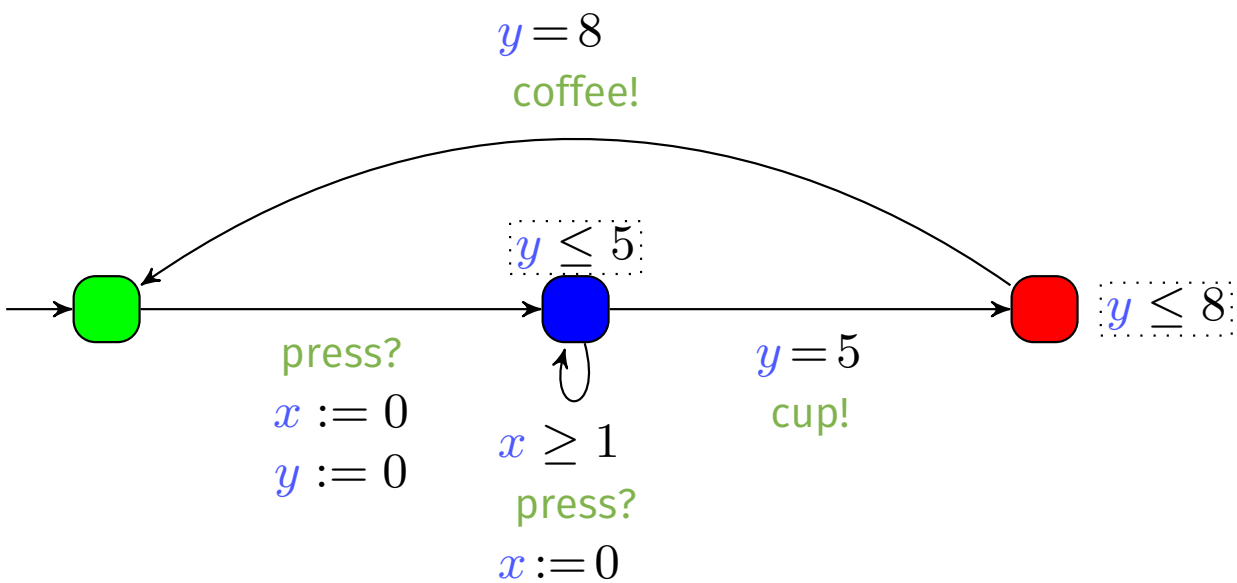
- Question: for what values of the parameters does the model of the system satisfy the property?

Yes if...

$$2\text{delay} > \text{period}$$
$$\wedge\ \text{period} < 20.46$$

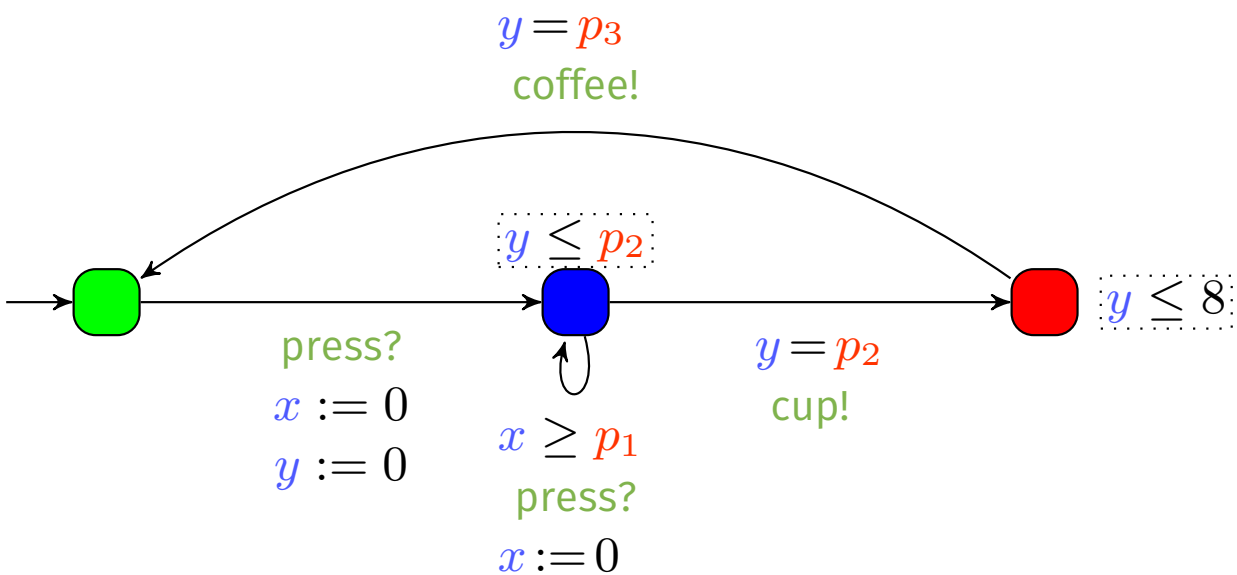
Parametric Timed Automaton (PTA)

- Timed automaton (sets of locations, actions and clocks)



Parametric Timed Automaton (PTA)

- Timed automaton (sets of locations, actions and clocks) augmented with a set P of parameters [Alur et al., 1993]
  - Unknown constants compared to a clock in guards and invariants



Notation: Valuation of a PTA

- Given a PTA $\mathcal{A}$ and a parameter valuation v, we denote by $v(\mathcal{A})$ the (non-parametric) timed automaton where each parameter p is valuated by $v(p)$

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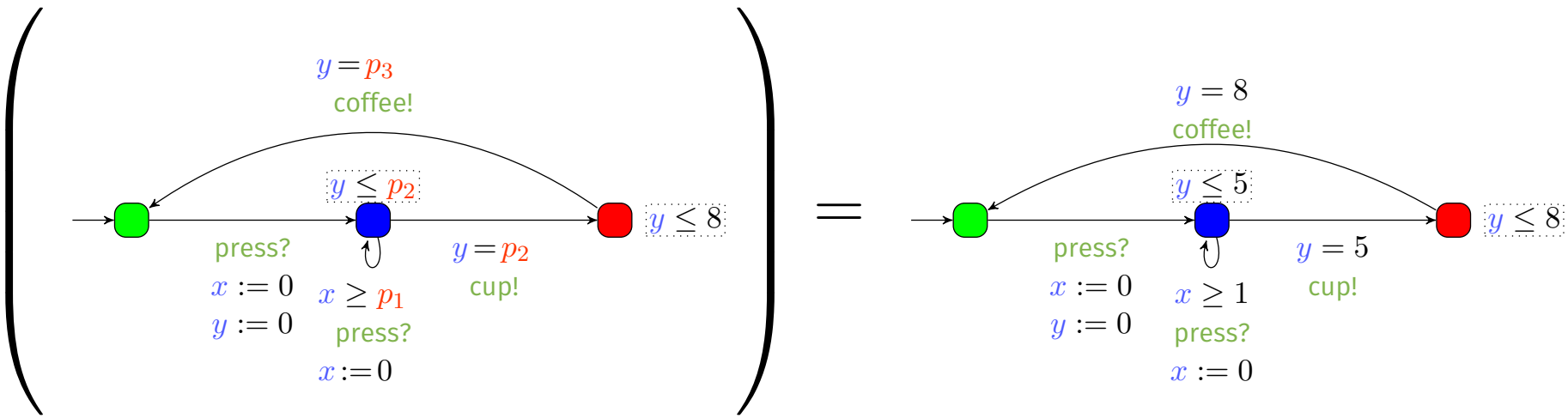
v



with v : $\begin{cases} p_1 & \rightarrow & 1 \\ p_2 & \rightarrow & 5 \\ p_3 & \rightarrow & 8 \end{cases}$

Symbolic semantics of parametric timed automata

- Symbolic state of a PTA: pair (l, C), where
  - l is a location,
  - C is a convex polyhedron over X and P with a special form, called parametric zone [Hune et al., 2002]

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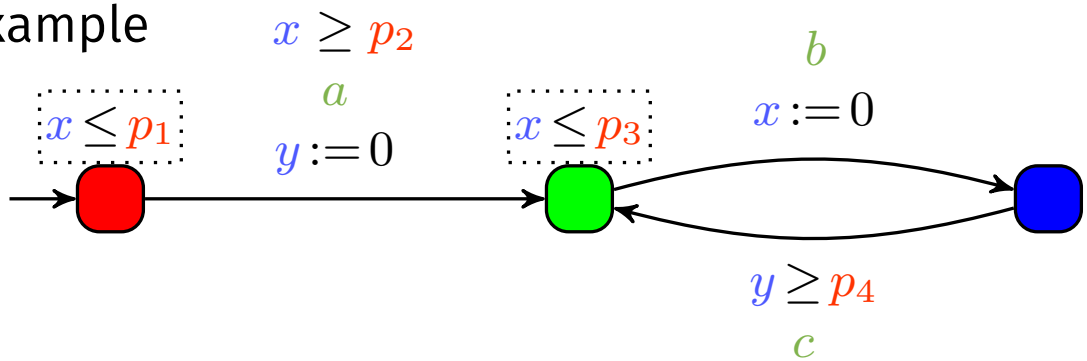
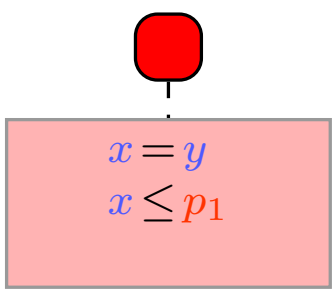


  - Possible symbolic run for this PTA



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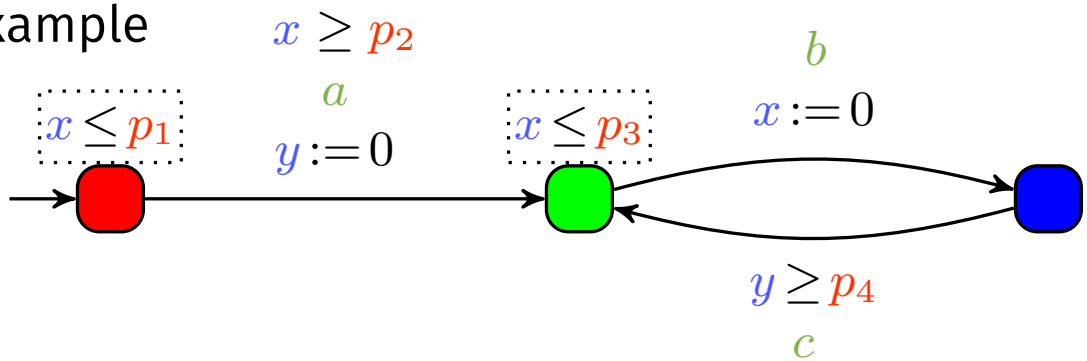

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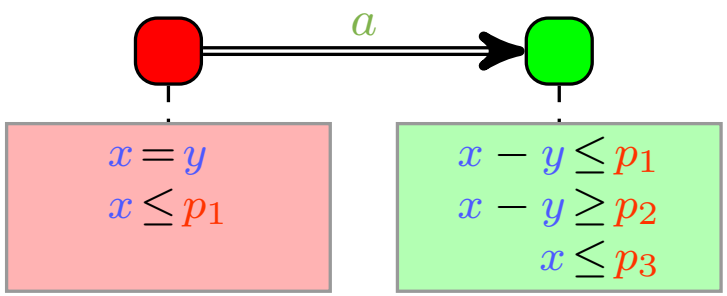

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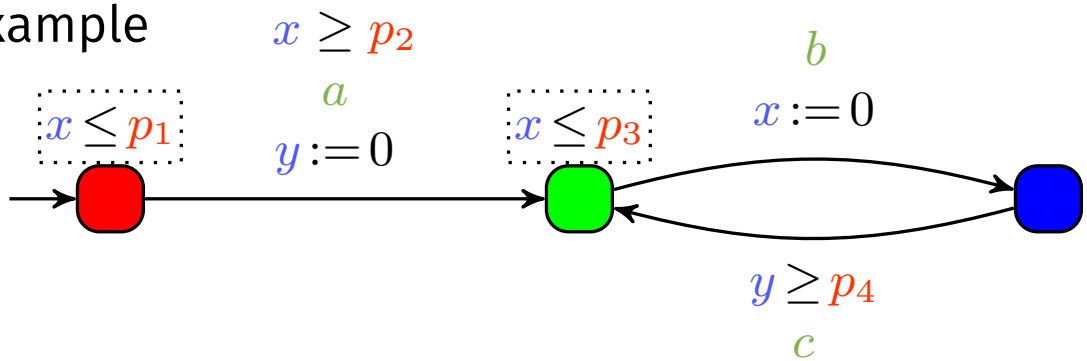

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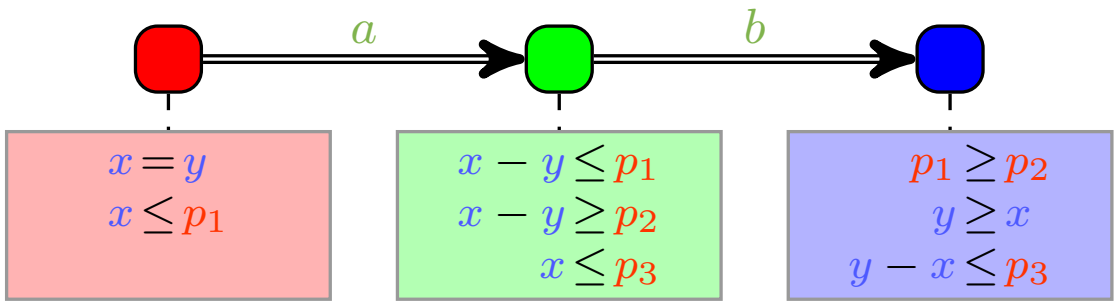
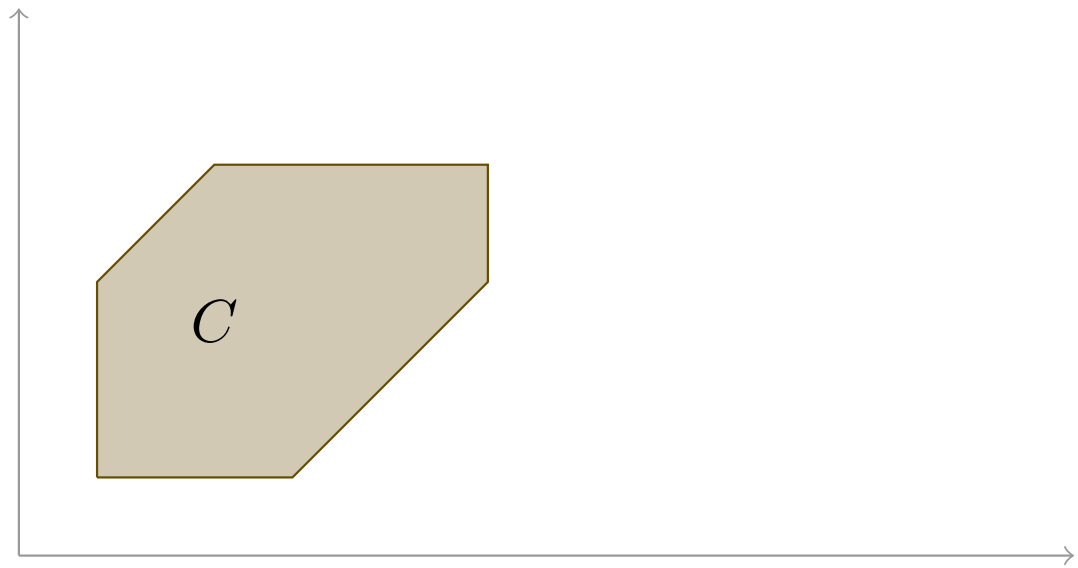


Symbolic semantics of PTA: Illustration

$$C' = [(C \cap g)]_R \cap I(l'))^{\nearrow} \cap I(l'))$$



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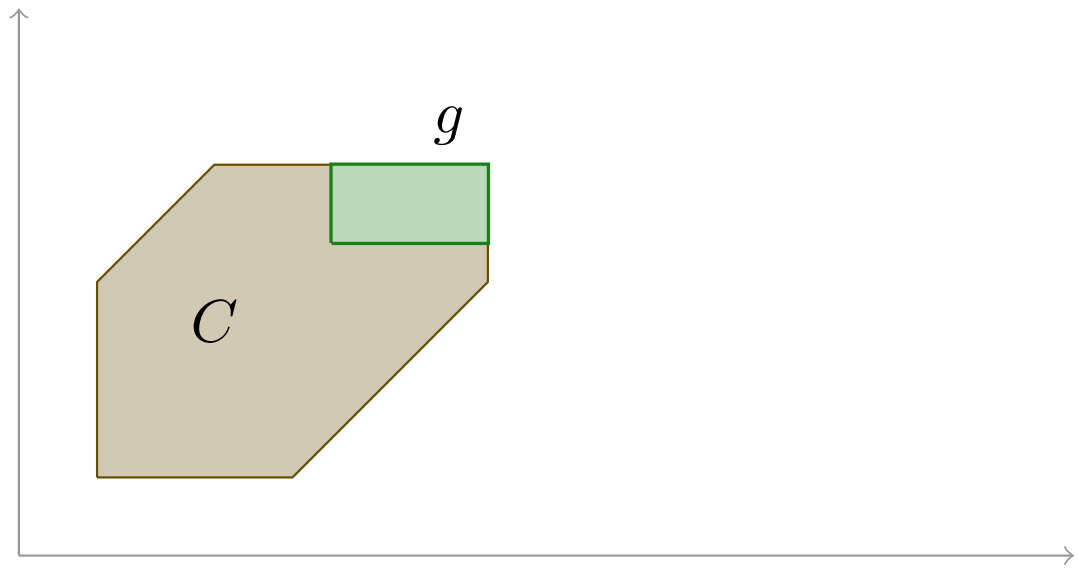

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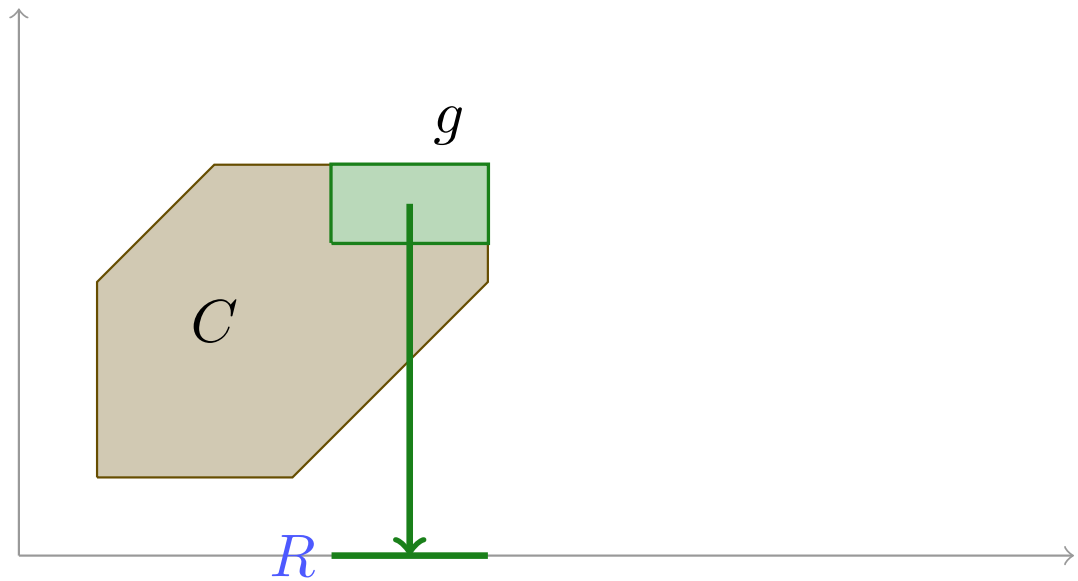

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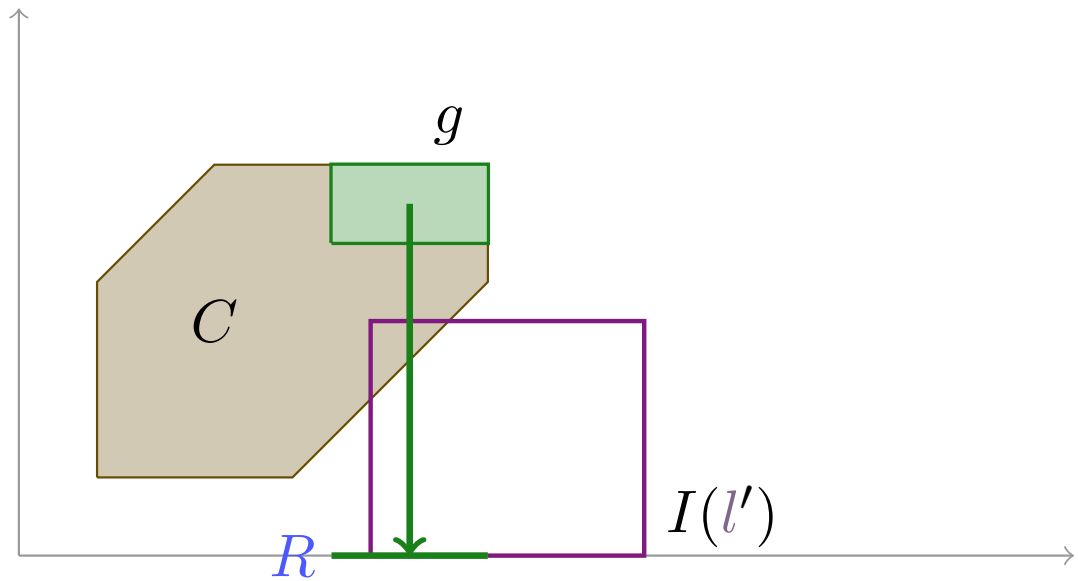

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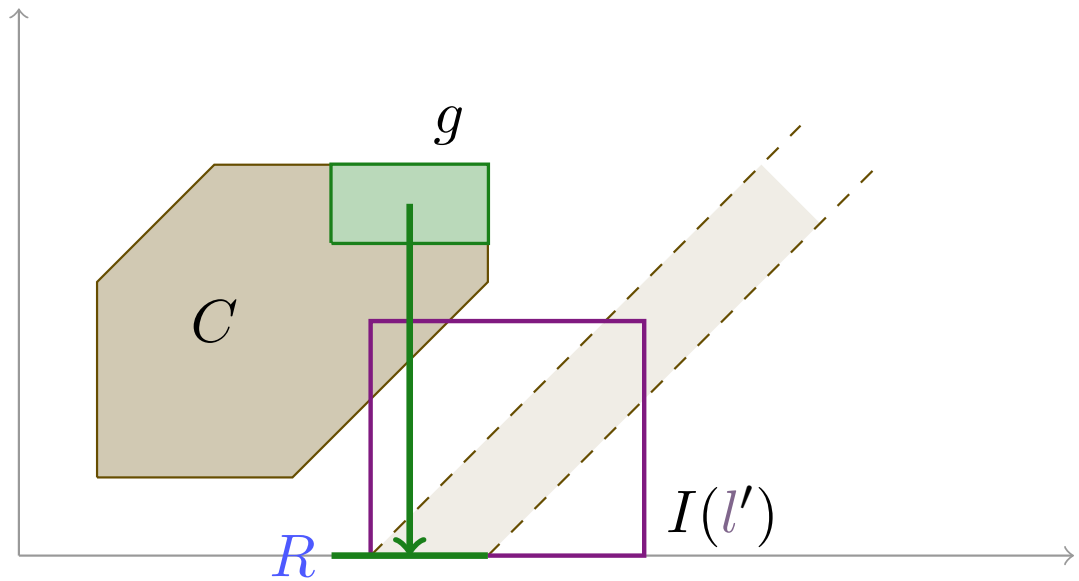

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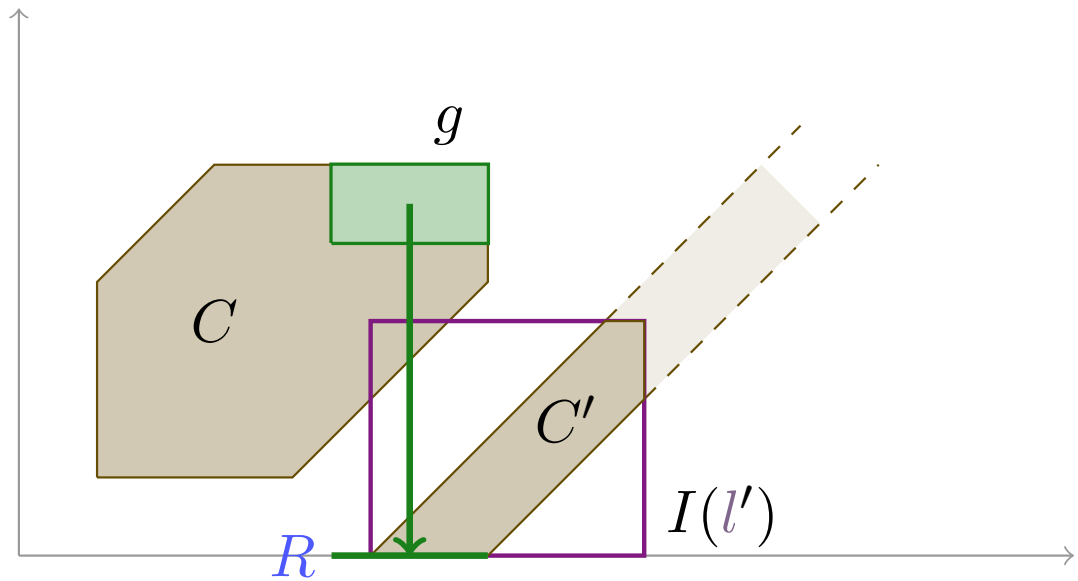

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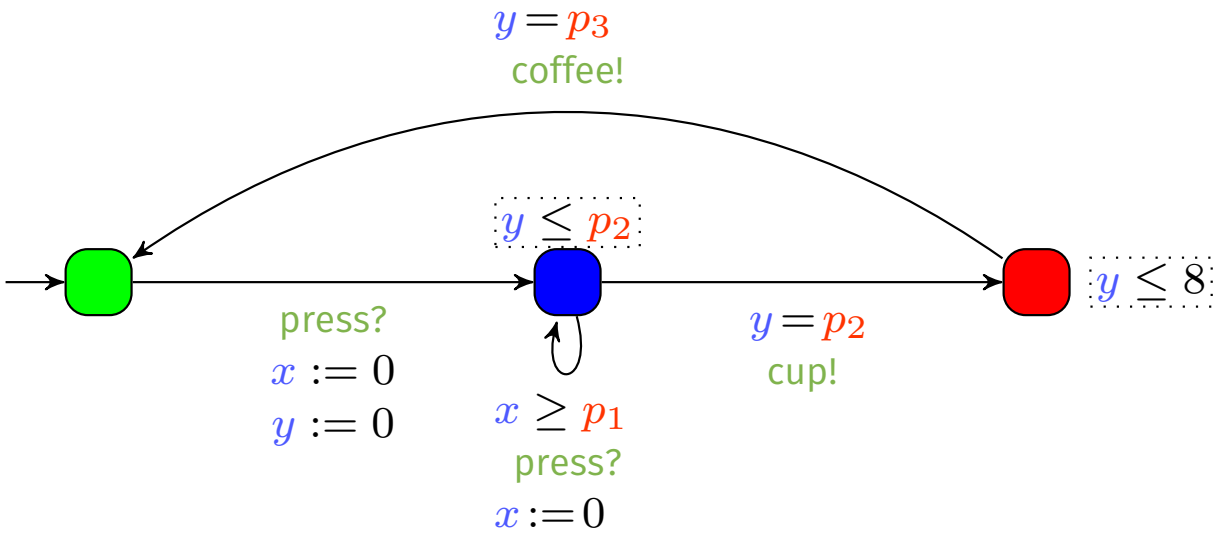

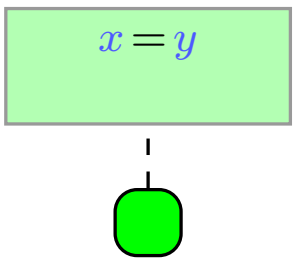

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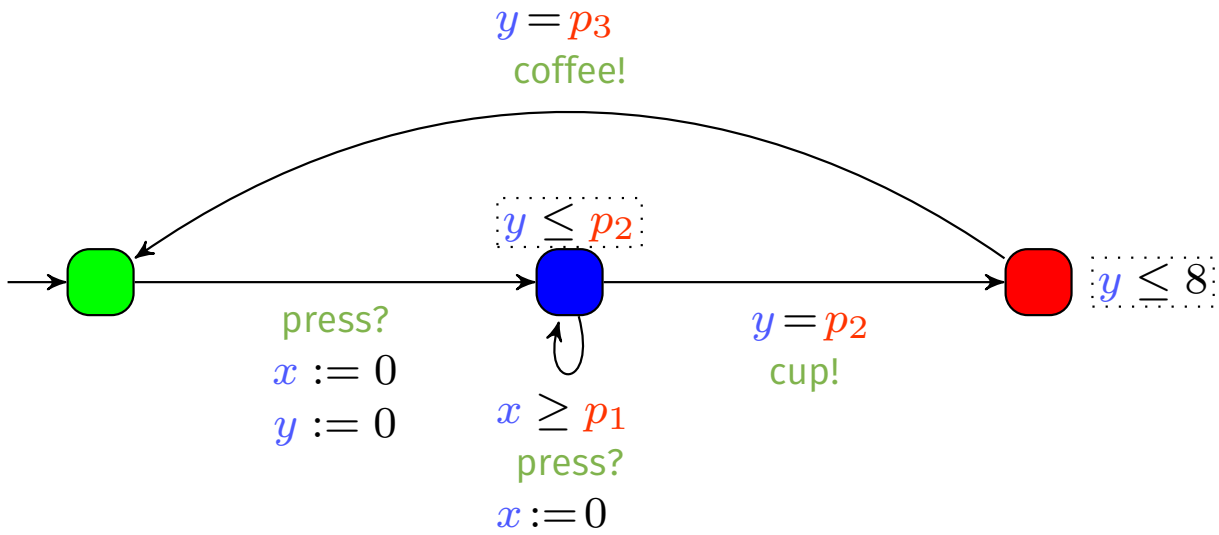

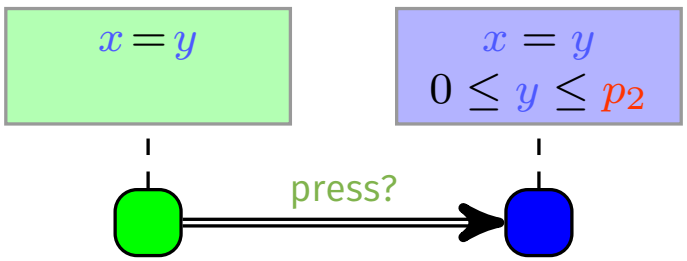

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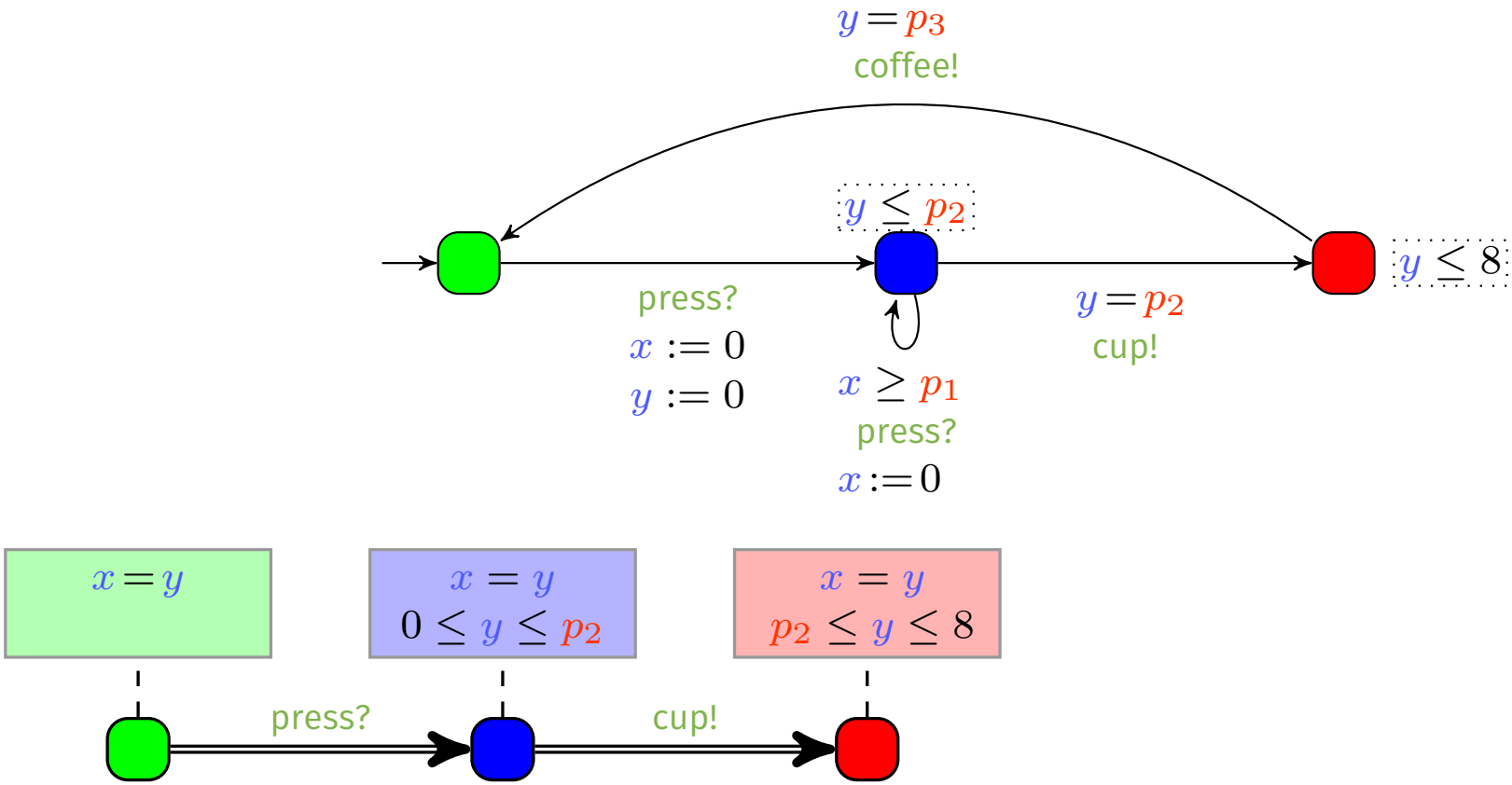

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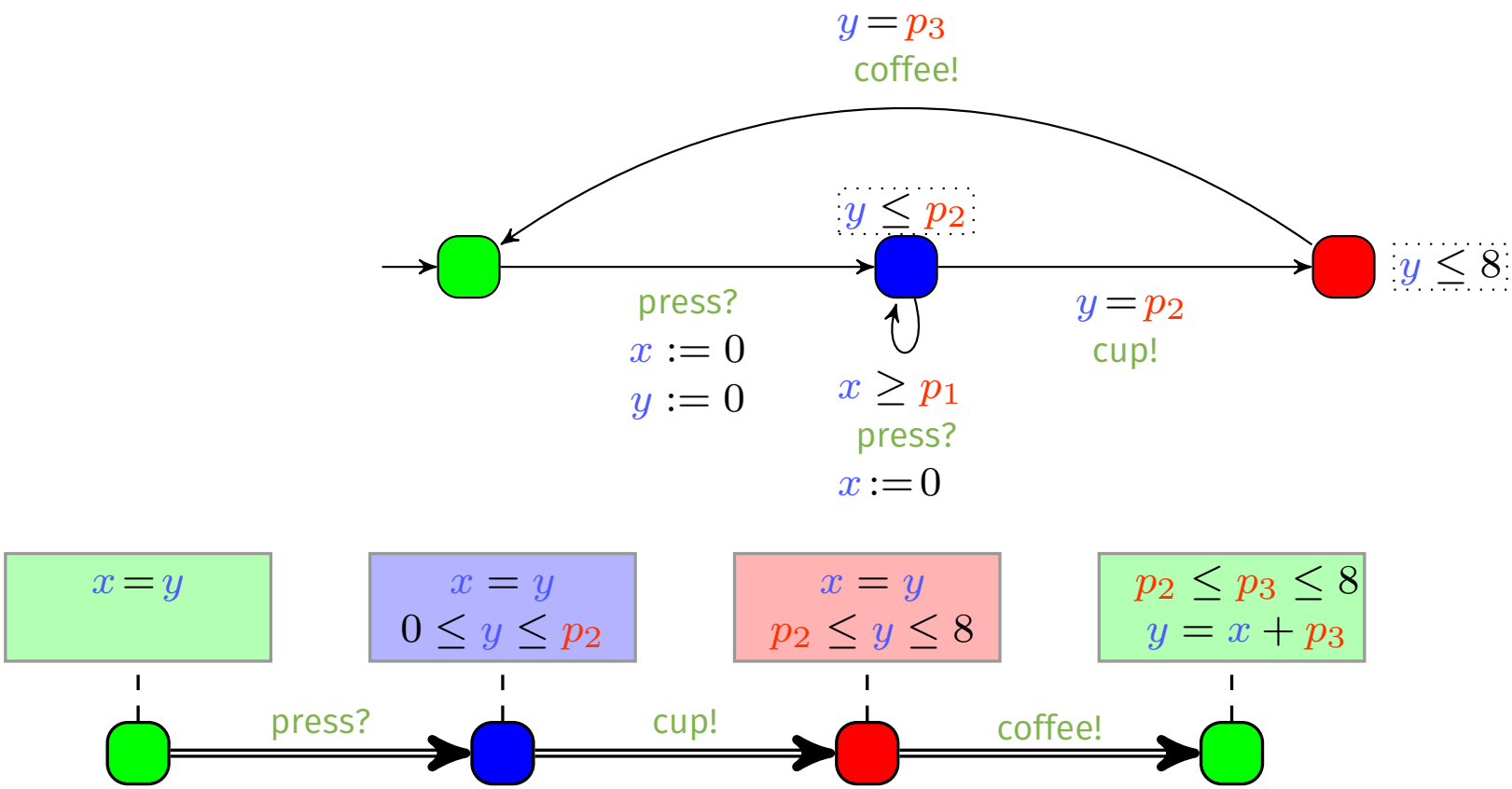

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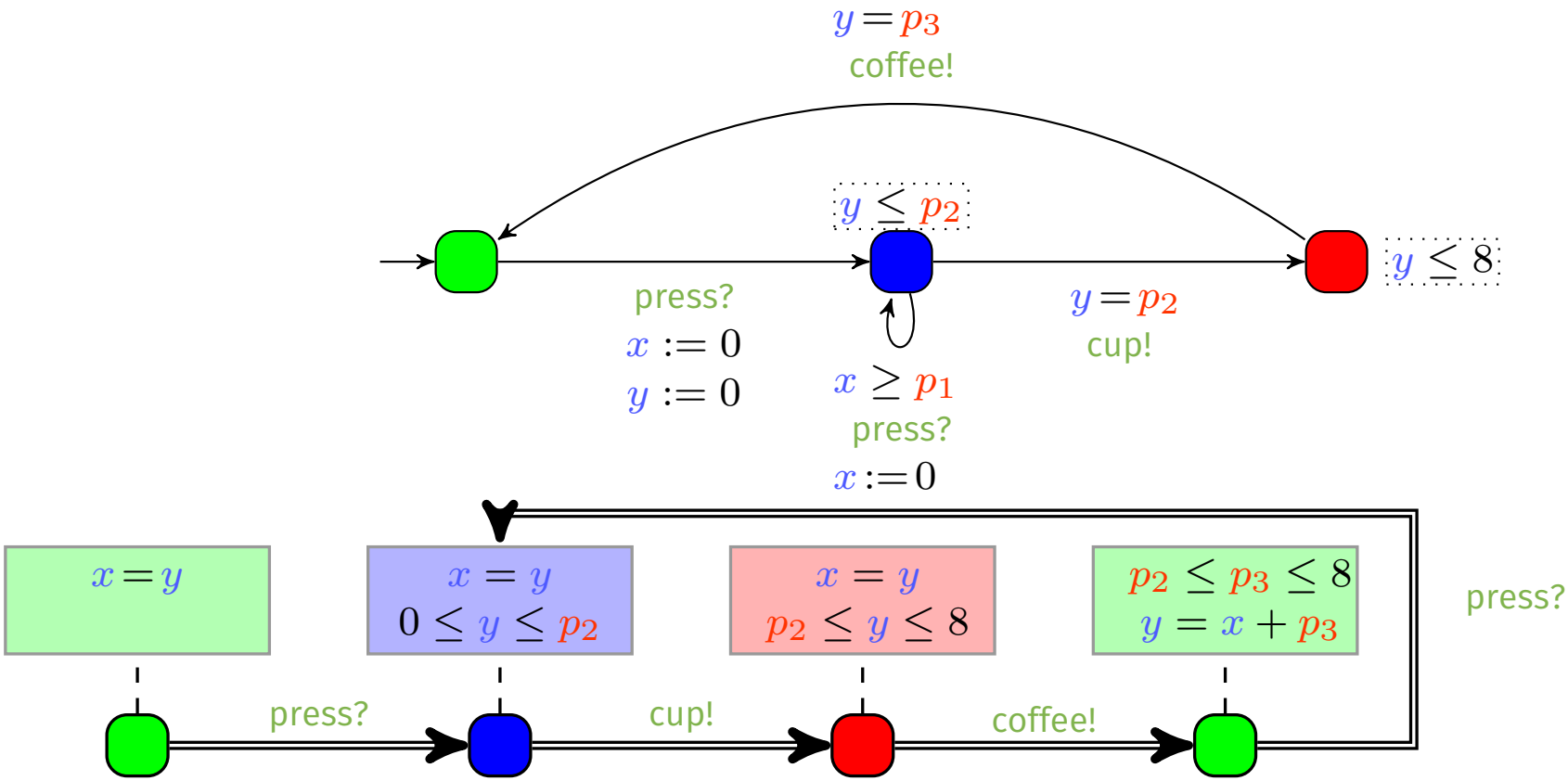

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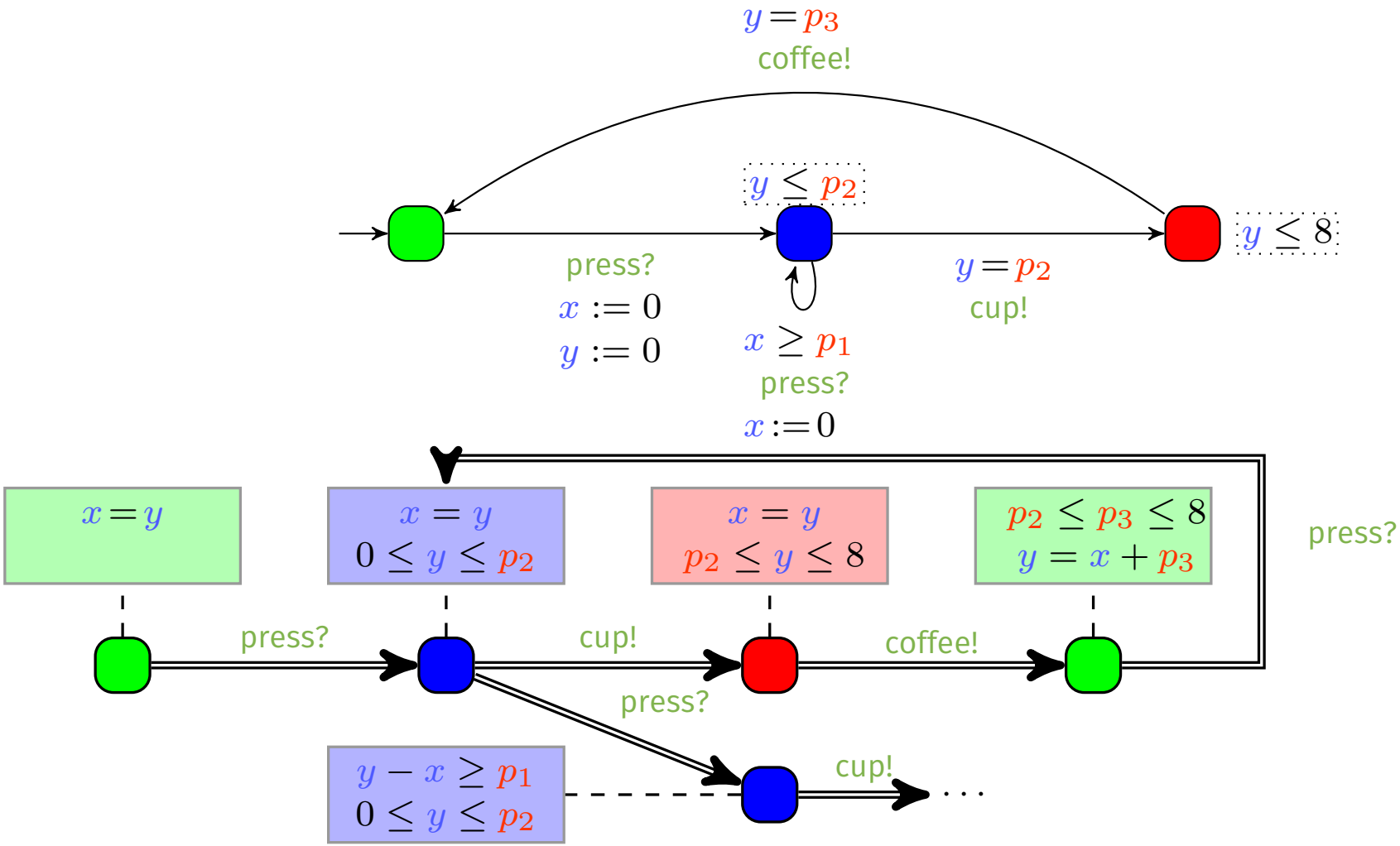

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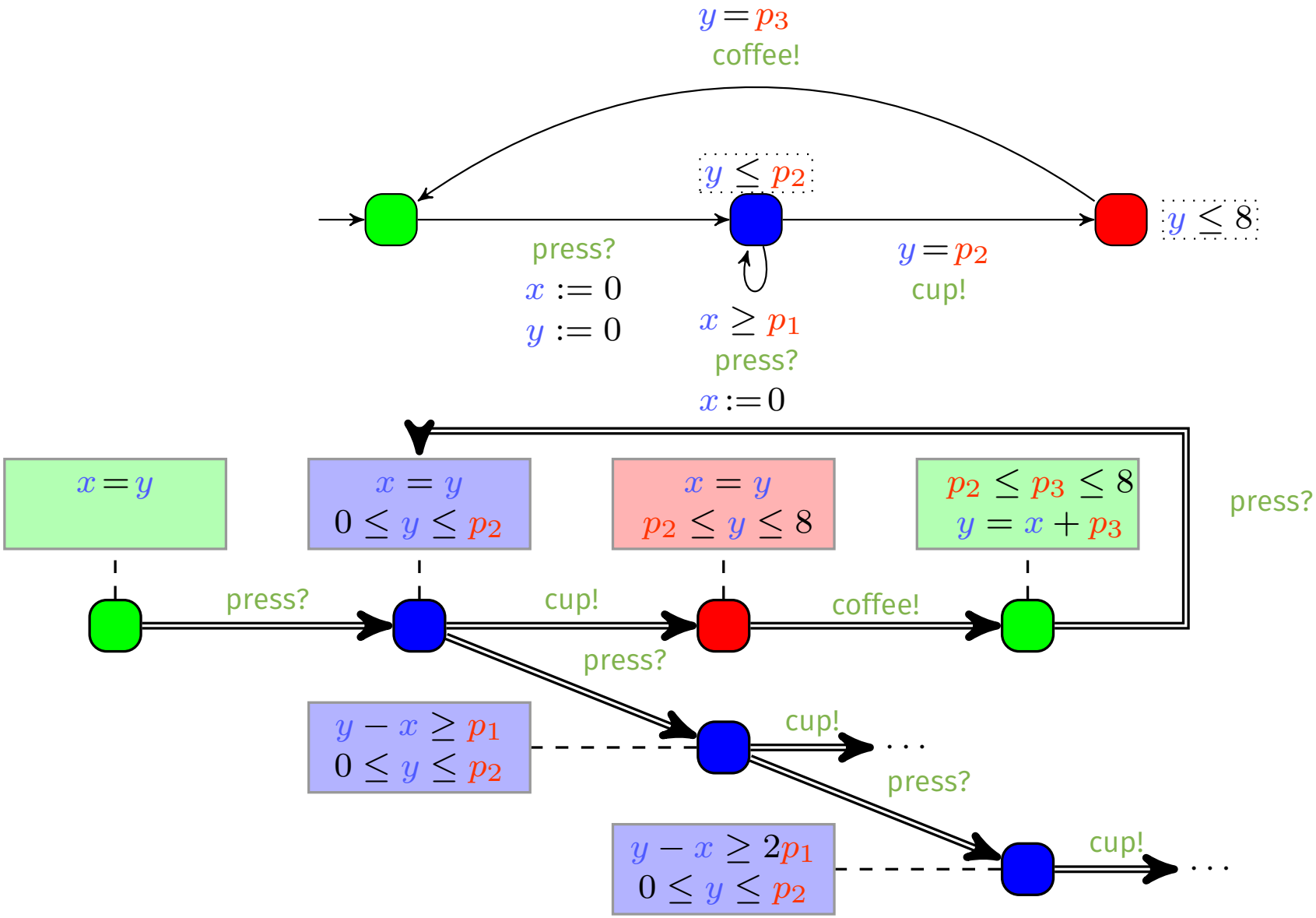

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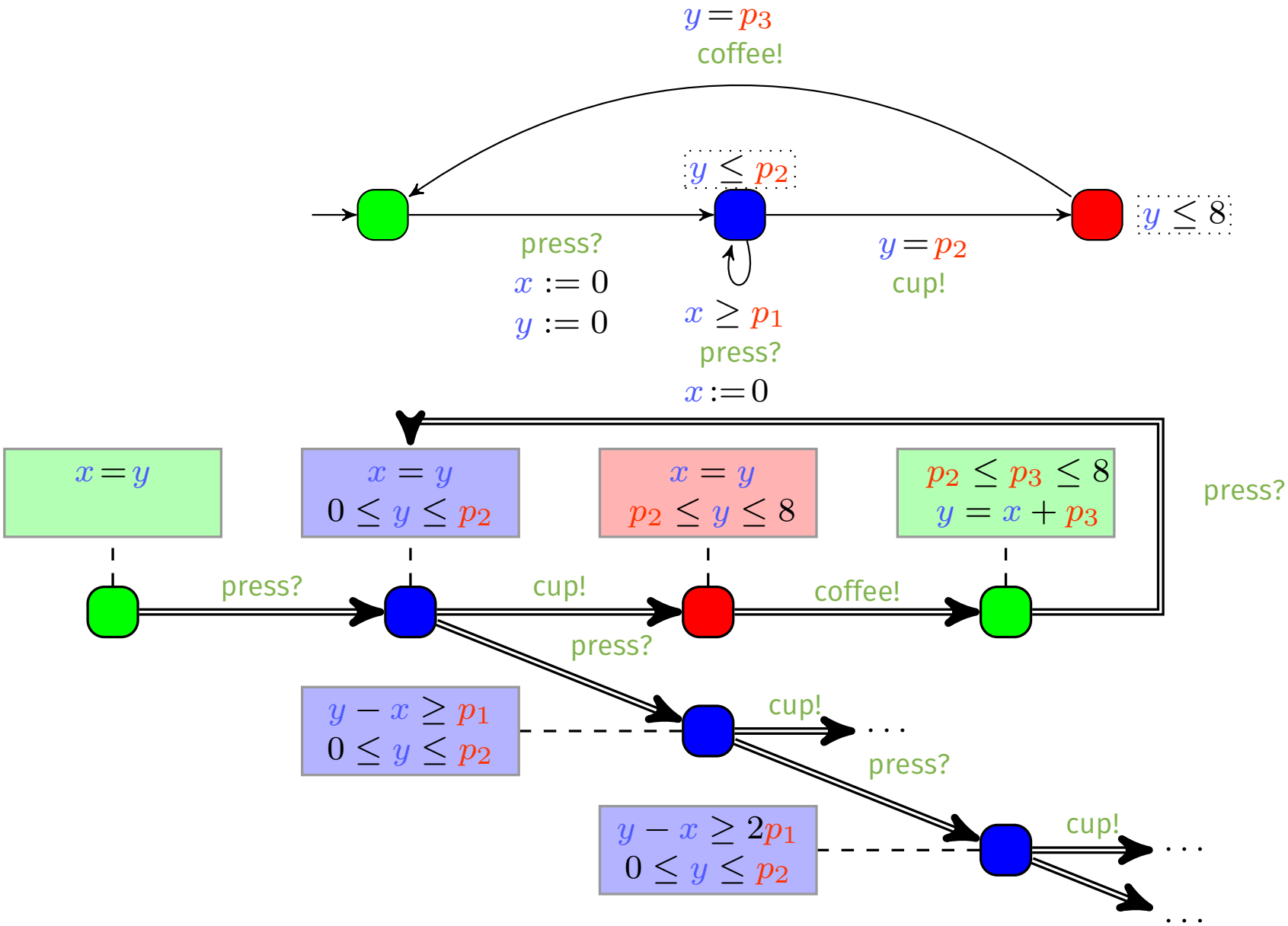

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If a decision problem is undecidable, it is hopeless to look for algorithms yielding exact solutions (because that is impossible)

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However, one can:

- design semi-algorithms: if the algorithm halts, then its result is correct
- design algorithms yielding over- or under-approximations

Decision and computation problems for PTA

- EF-Emptiness "Is the set of parameter valuations for which a given location l is reachable empty?"

  Example: "Does there exist at least one parameter valuation for which I can get a coffee with 2 sugars?"

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- The symbolic state space is infinite in general
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Bad news

All interesting problems are undecidable for (general) parametric timed automata.

[ÉA, STTT 2017]

Undecidability in a nutshell

- EF-emptiness problem

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- Preservation of the untimed language
  "Given a parameter valuation, does there exist another valuations with the same untimed language?" [André and Markey, 2015]

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Restraining the syntax brings decidability of some problems:

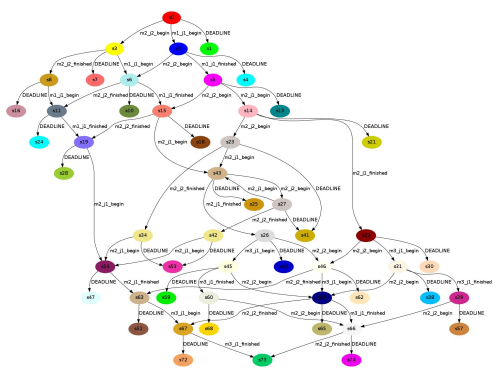
- L/U-PTAs [Hune et al., 2002, Bozzelli and La Torre, 2009, André and Markey, 2015, André and Lime, 2017, André et al., 2018b]
- PTAs with bounded integer-valued parameters [Jovanović et al., 2015]
- reset-PTAs [André et al., 2016, André et al., 2018c]

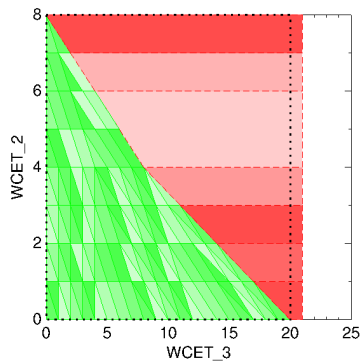
Outline

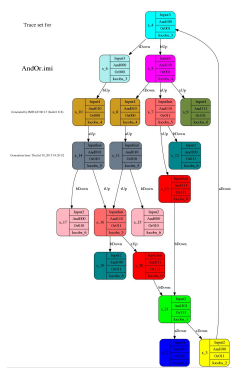
IMITATOR

- A tool for modeling and verifying timed concurrent systems with unknown constants modeled with parametric timed automata
  - Communication through (strong) broadcast synchronization
  - Rational-valued shared discrete variables
  - Stopwatches, to model schedulability problems with preemption

- Synthesis algorithms
  - (non-Zeno) parametric model checking (using a subset of TCTL)
  - Language and trace preservation, and robustness analysis
  - Parametric deadlock-freeness checking







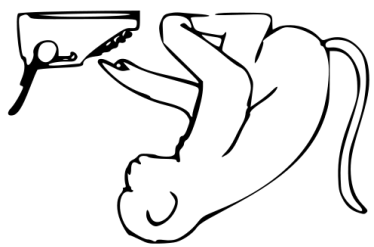
IMITATOR

Under continuous development since 2008 [André et al., FM'12]

A library of benchmarks

- Communication protocols
- Schedulability problems
- Asynchronous circuits
- …and more

Free and open source software: Available under the GNU-GPL license



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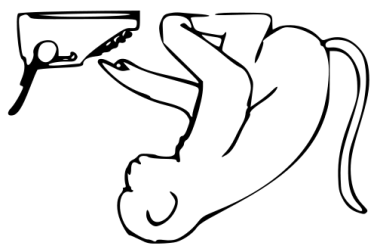

Try it!

www.imitator.fr

Some success stories

- Modeled and verified an asynchronous memory circuit by ST-Microelectronics
- Parametric schedulability analysis of a prospective architecture for the flight control system of the next generation of spacecrafts designed at ASTRIUM Space Transportation [Fribourg et al., 2012]
- Verification of software product lines [Luthmann et al., 2017]
- Offline monitoring [ÉA, Hasuo, Waga @ ICECCS'18]
- Formal timing analysis of music scores [Fanchon and Jacquemard, 2013]
- Solution to a challenge related to a distributed video processing system by Thales

Outline

Modeling real-time systems with timed automata

- Using timed automata
  - [Abdeddaïm and Maler, 2001]
- Using stopwatch automata
  - [Adbeddaïm and Maler, 2002]
- Using parametric timed automata
  - [Cimatti et al., 2008]
- Using parametric stopwatch automata
  - [Fribourg et al., 2012, Sun et al., 2013, Lipari et al., 2014]
- Using task automata
  - [Norström et al., 1999, Fersman et al., 2007, André, 2017]

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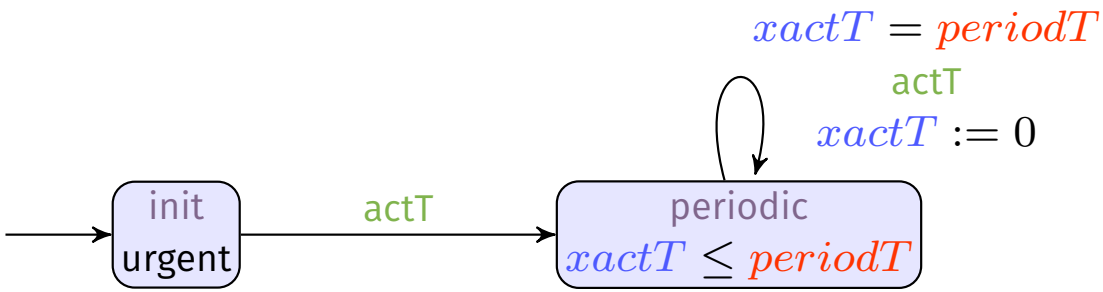

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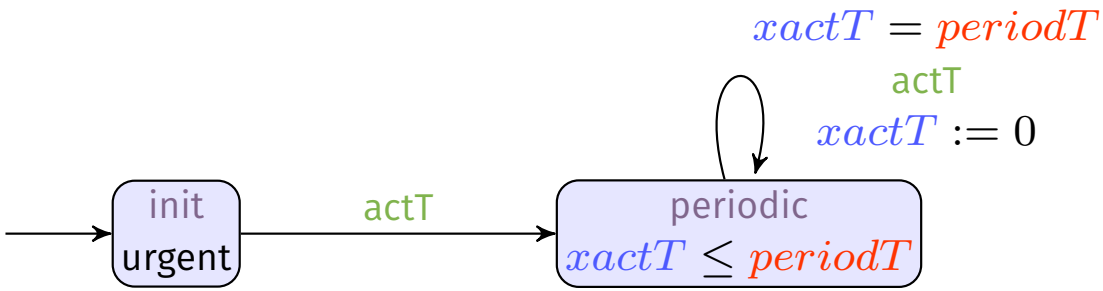

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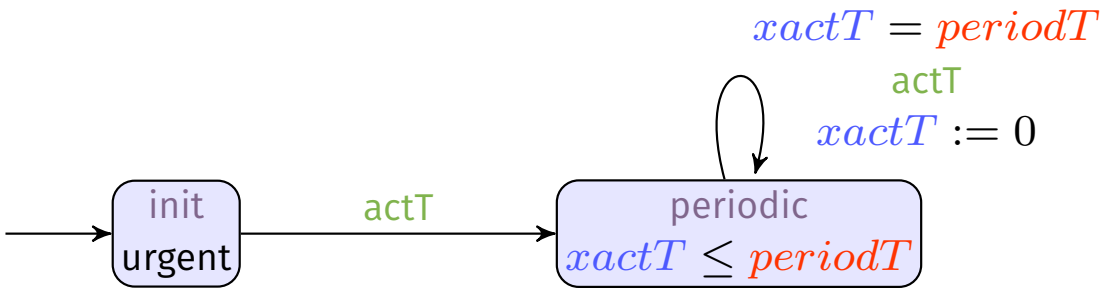

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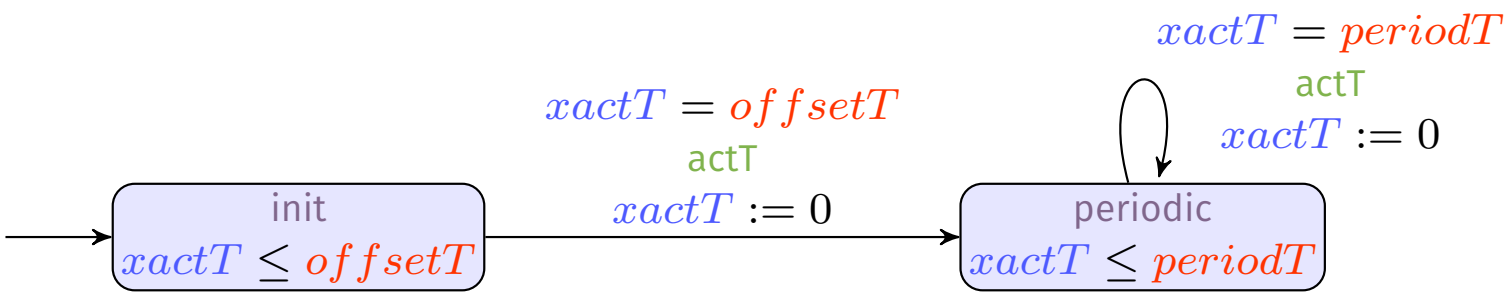

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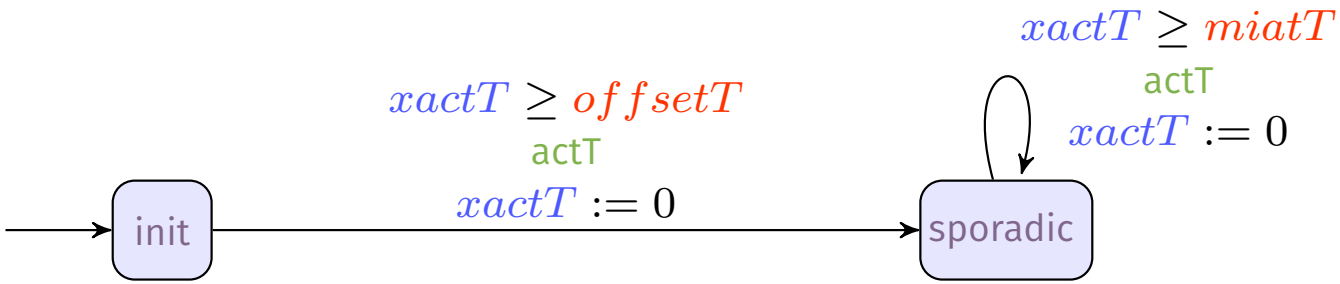

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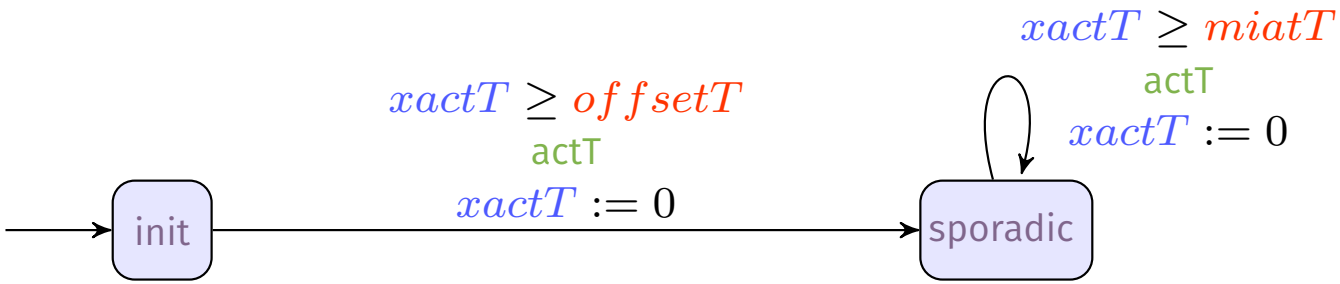

A more efficient modeling to avoid clock divergence in IMITATOR

- and hence optimize the computation

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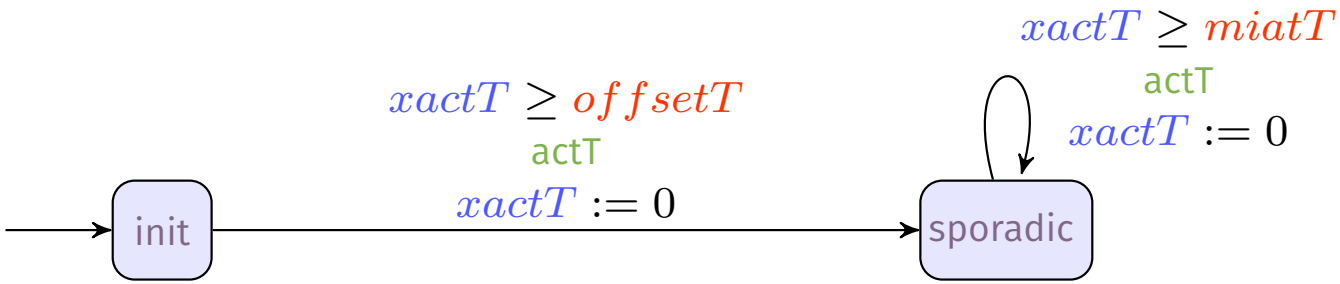

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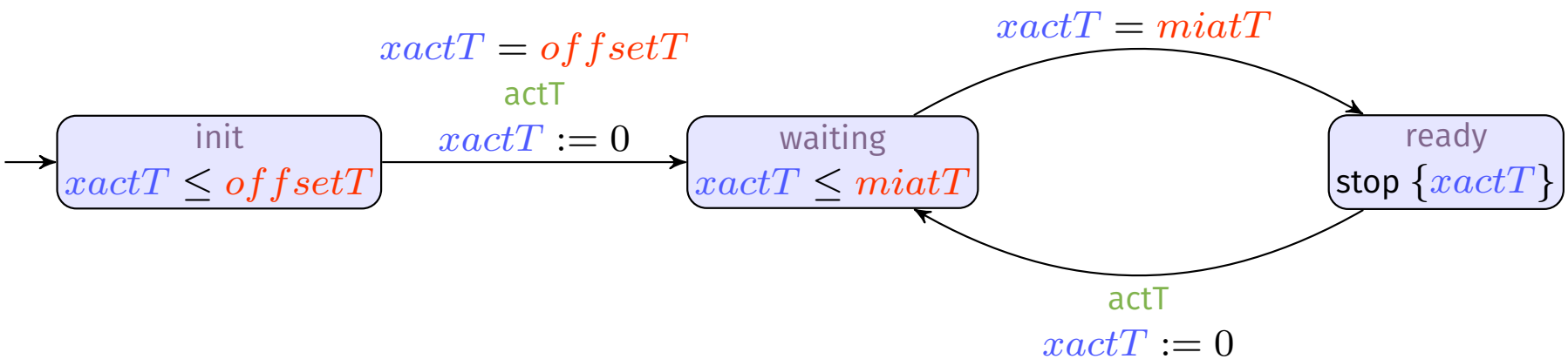

Trick: stop the computation of $xactT$ to avoid diverging

Modeling a task / pipeline

Pipeline P of two tasks T_1 and T_2

The pipeline has a period $periodP$

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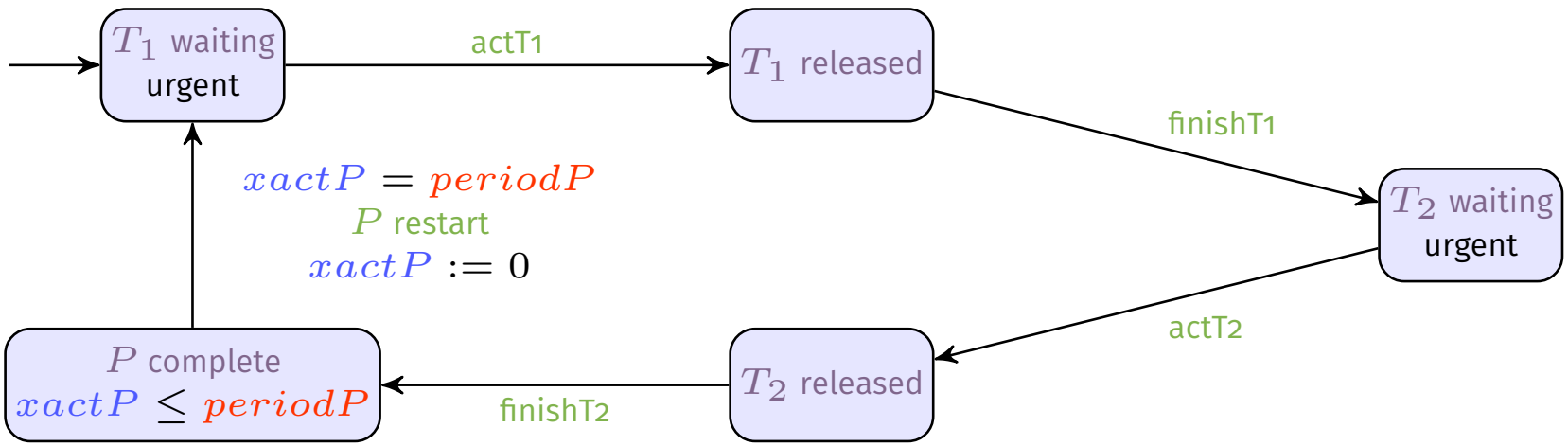
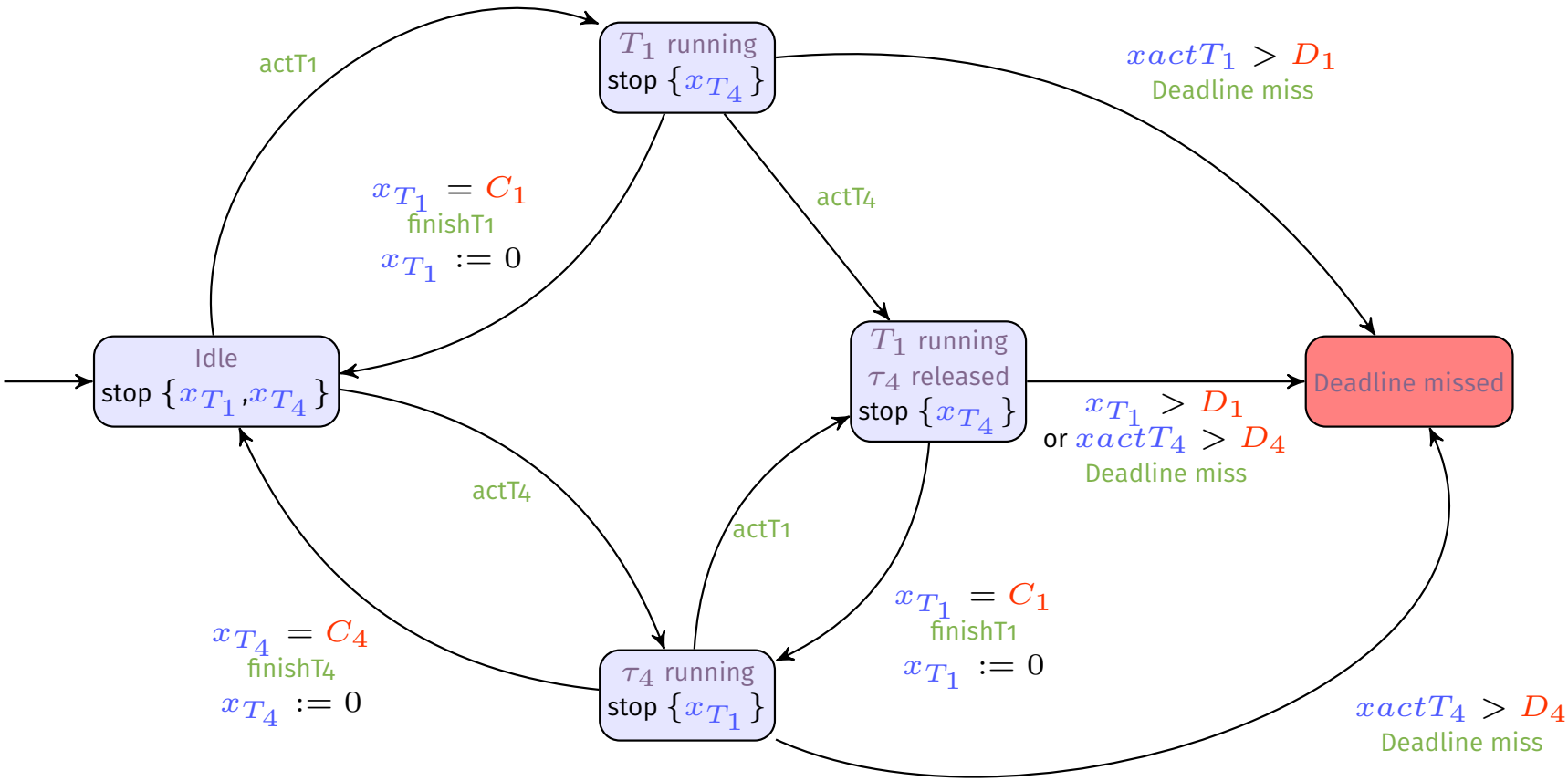


Modeling the preemptive fixed priority scheduler

A fixed-priority preemptive processor with two tasks T_1 and T_4

Timings for T_1: period $periodT1$, execution time period C_1, deadline period D_1

- and similarly for T_4



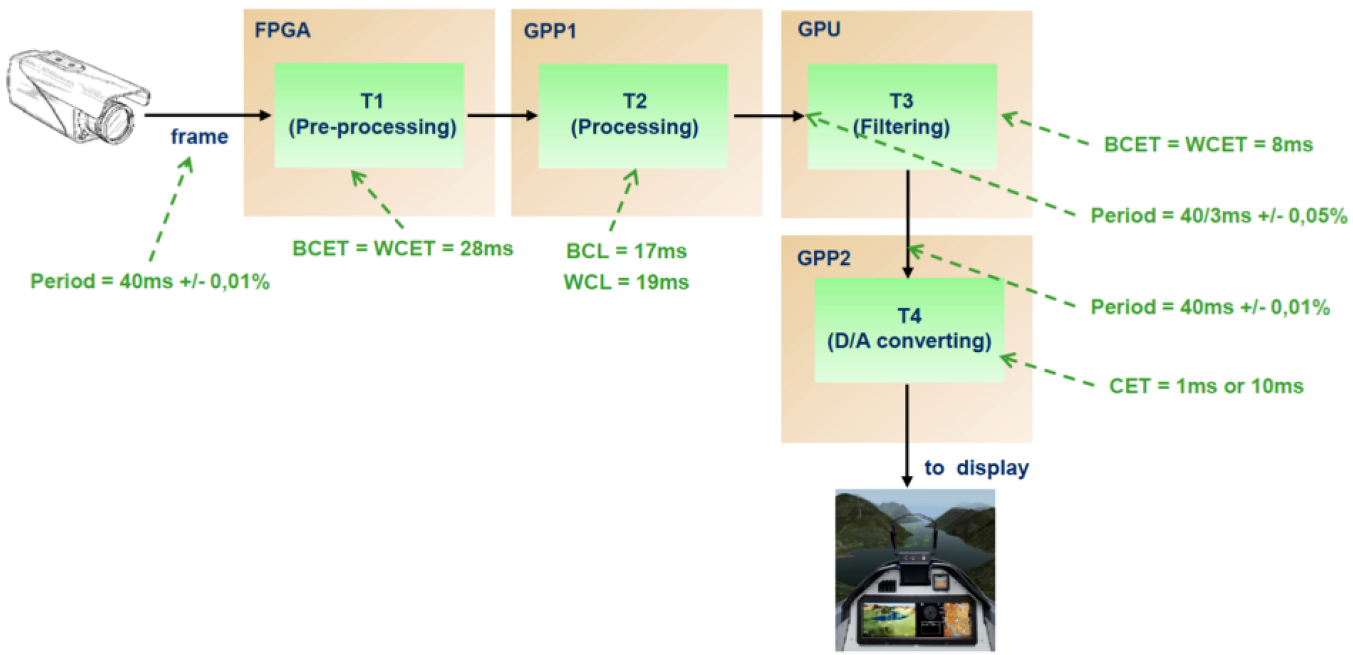
Outline

The FMTV 2015 Challenge (1/2)

Challenge by Thales proposed during the WATERS 2014 workshop
Solutions presented at WATERS 2015

System: an unmanned aerial video system with uncertain periods

- Period constant but with a small uncertainty (typically 0.01 %)
- Not a jitter!



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Compute the end-to-end BCET and WCET times for a buffer size of $n = 1$ and $n = 3$

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Compute the end-to-end BCET and WCET times for a buffer size of $n = 1$ and $n = 3$

☹ Not a typical parameter synthesis problem?

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☺ A typical parameter synthesis problem

- The end-to-end time can be set as a parameter… to be synthesized
- The uncertain period is typically a parameter (with some constraint, e. g., $P1 \in [40 - 0.004, 40 + 0.004]$)

Methodology

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5. Eliminate all parameters but the end-to-end time

Note: not eliminating parameters allows one to know for which values of the periods the best / worst case execution times are obtained.

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2. Add a specific location corresponding to the correct transmission of the frame
3. Run the reachability synthesis algorithm EFsynth (implemented in IMITATOR) w.r.t. that location
4. Gather all constraints (in as many dimensions as uncertain periods + the end-to-end time)
5. Eliminate all parameters but the end-to-end time
6. Exhibit the minimum and the maximum

Note: not eliminating parameters allows one to know for which values of the periods the best / worst case execution times are obtained.

To build the PTA model

- Uncertainties in the system:
  - $P1 \in [40 - 0.004, 40 + 0.004]$
  - $P3 \in [\frac{40}{3} - \frac{1}{150}, \frac{40}{3} + \frac{1}{150}]$
  - $P4 \in [40 - 0.004, 40 + 0.004]$

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  - $P1 \in [40 - 0.004, 40 + 0.004]$
  - $P3 \in [\frac{40}{3} - \frac{1}{150}, \frac{40}{3} + \frac{1}{150}]$
  - $P4 \in [40 - 0.004, 40 + 0.004]$
- Parameters:
  - P1_uncertain
  - P3_uncertain
  - P4_uncertain

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  - $P4 \in [40 - 0.004, 40 + 0.004]$
- Parameters:
  - $\mathrm{P1\_uncertain}$
  - $\mathrm{P3\_uncertain}$
  - $\mathrm{P4\_uncertain}$
- The end-to-end latency (another parameter): $\mathrm{E2E}$

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  - $P1 \in [40 - 0.004, 40 + 0.004]$
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  - $P4 \in [40 - 0.004, 40 + 0.004]$
- Parameters:
  - $\mathrm{P1\_uncertain}$
  - $\mathrm{P3\_uncertain}$
  - $\mathrm{P4\_uncertain}$
- The end-to-end latency (another parameter): $\mathrm{E2E}$
- Others:
  - the register between task 2 and task 3: discrete variable $\mathrm{reg}_{2,3}$
  - the buffer between task 3 and task 4: $n = 1$ or $n = 3$

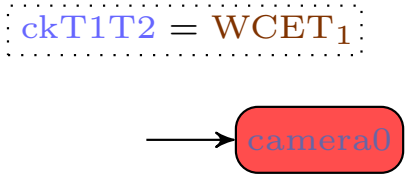
Simplification

- T1 and T2 are synchronised; T1, T3 and T4 are asynchronised
  - (exact modeling of the system behaviour is too heavy)

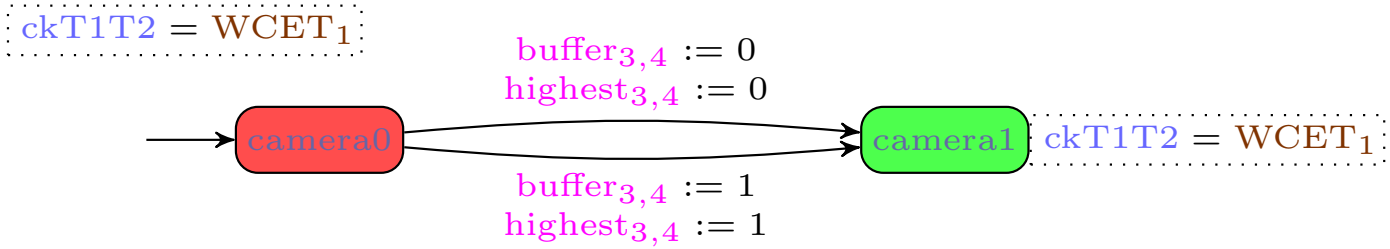
Simplification

- T1 and T2 are synchronised; T1, T3 and T4 are asynchronised
  - (exact modeling of the system behaviour is too heavy)
- We choose a single arbitrary frame, called the target one
- We assume the system is initially in an arbitrary status
  - This is our only uncertain assumption (in other words, can the periods deviate from each other so as to yield any arbitrary deviation?)

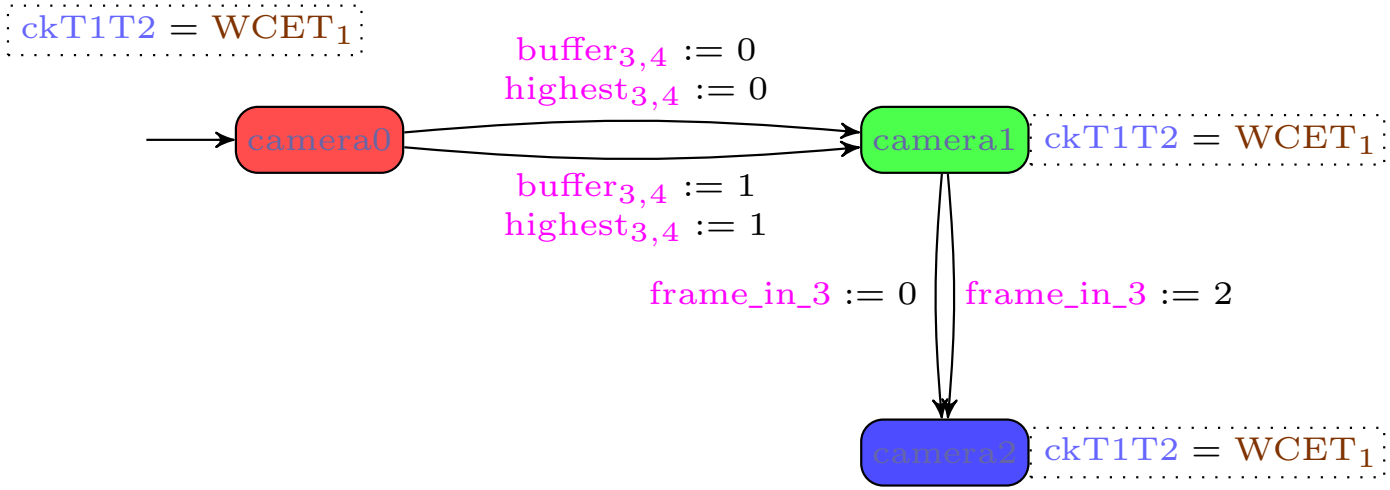
The initialization automaton



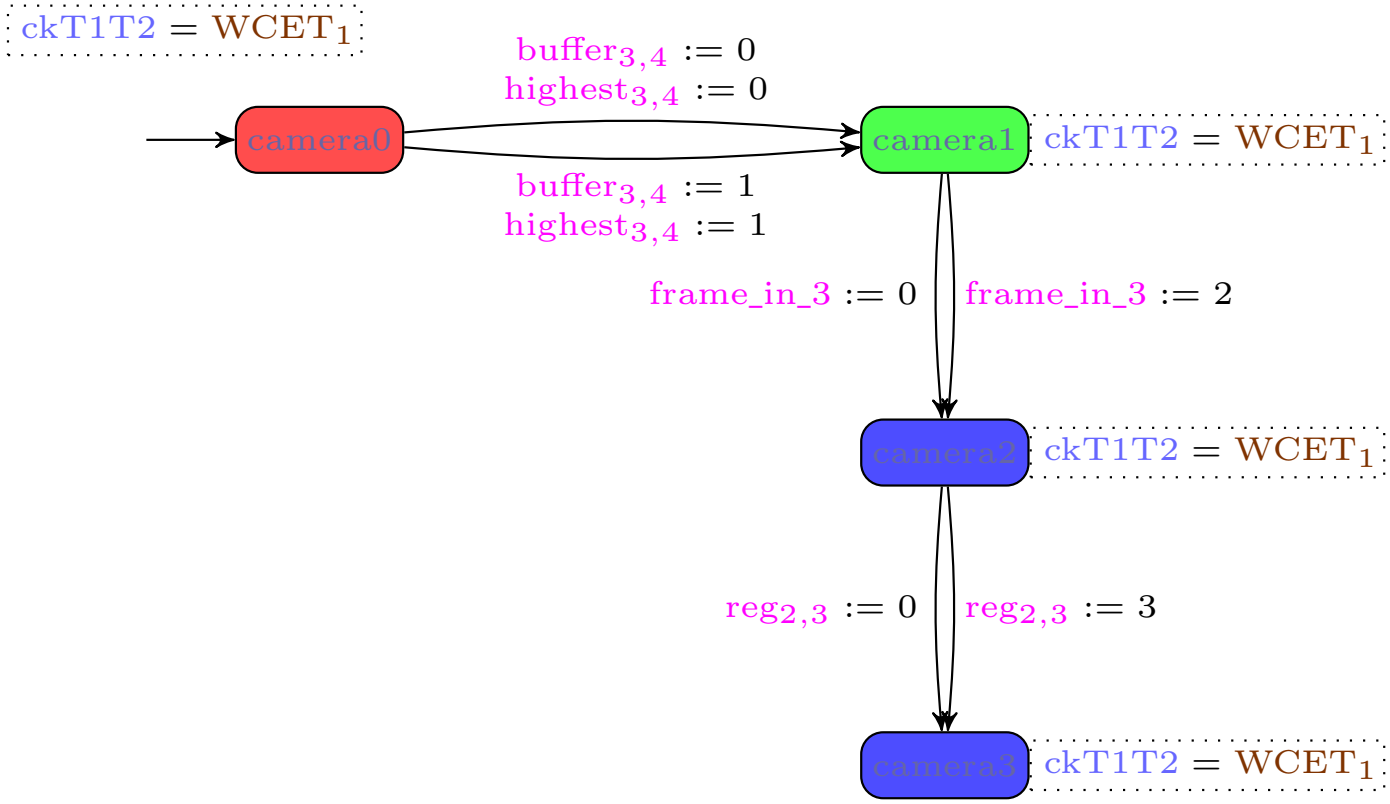
The initialization automaton



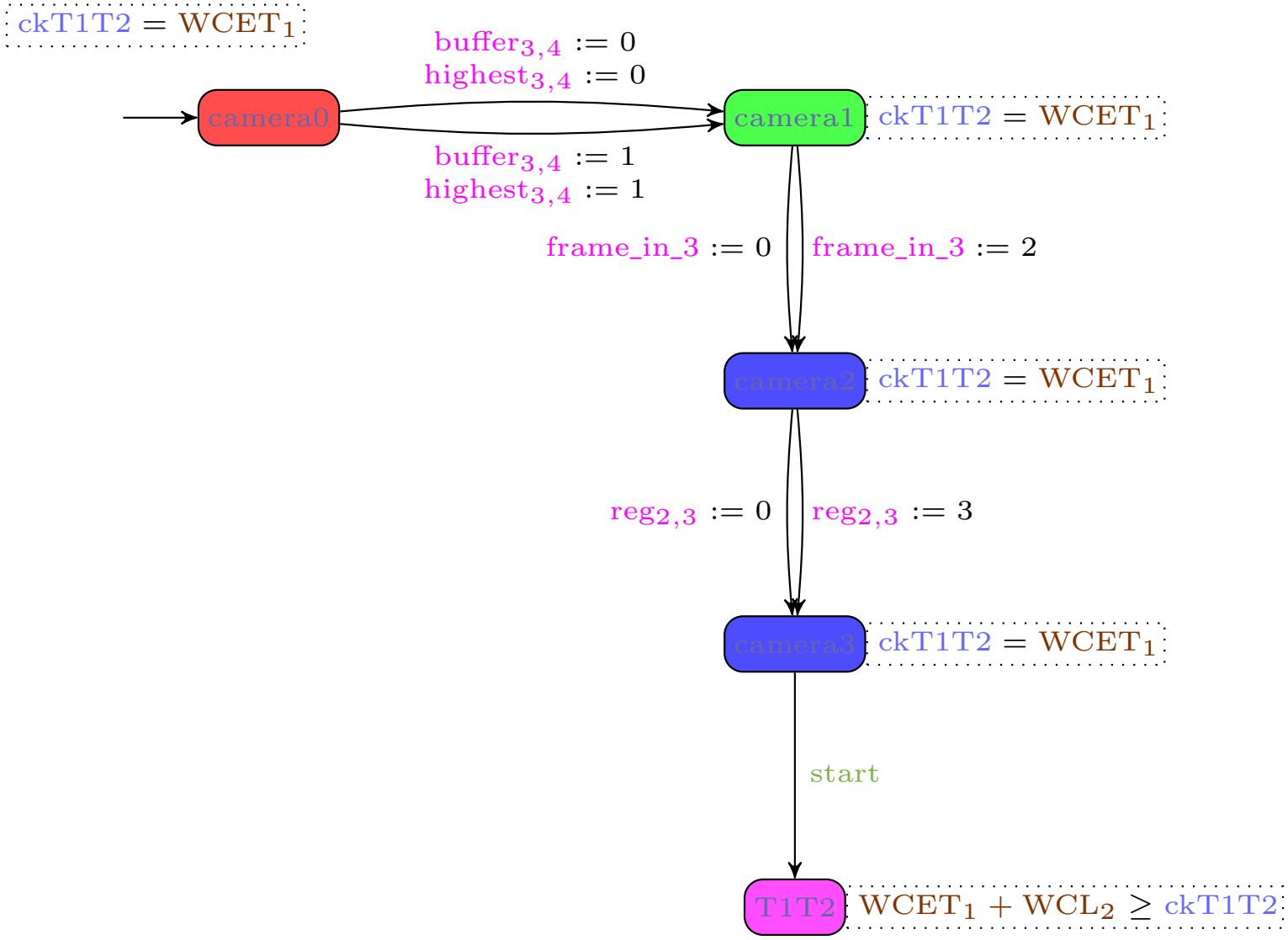
The initialization automaton



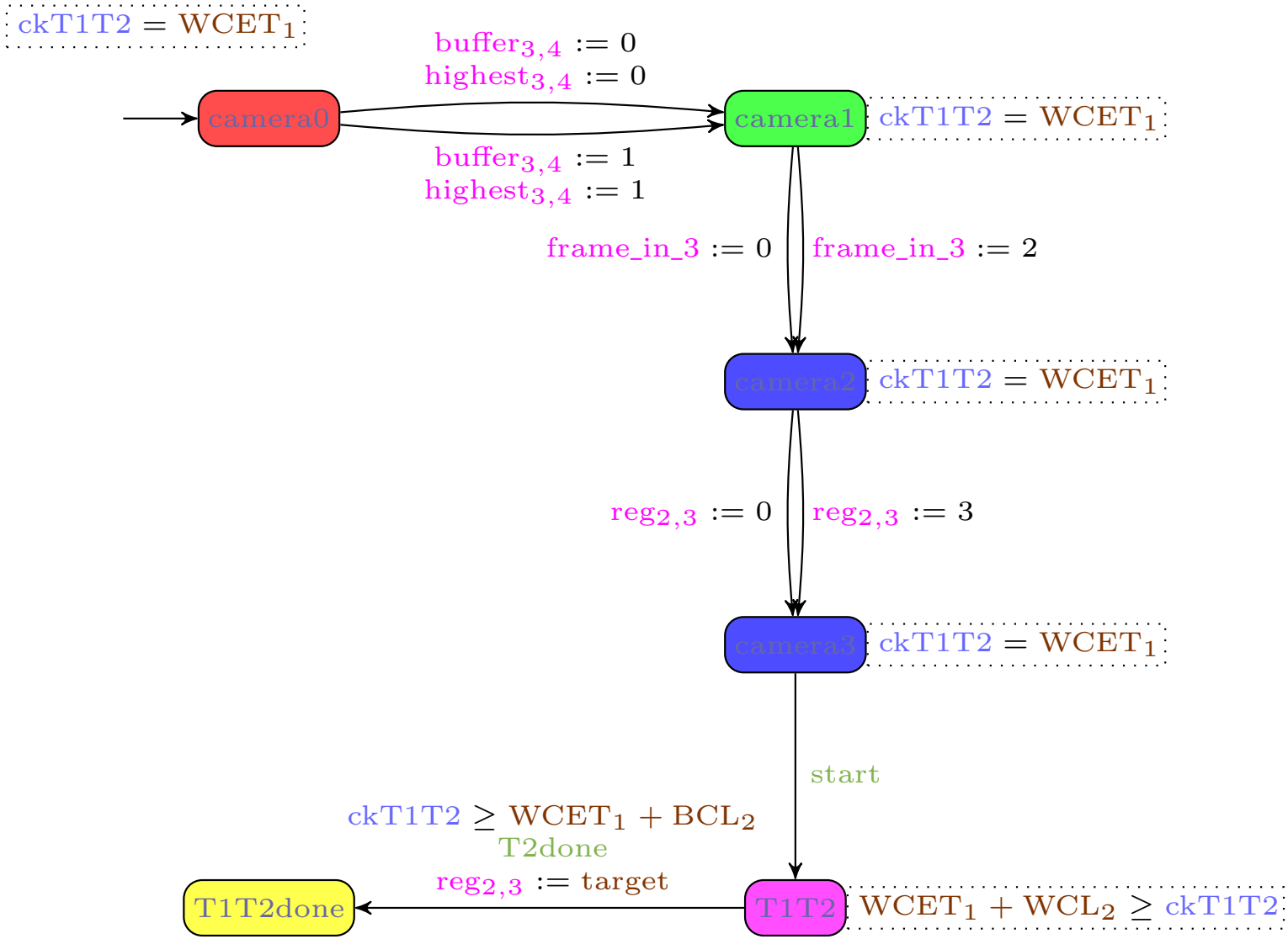
The initialization automaton



The initialization automaton

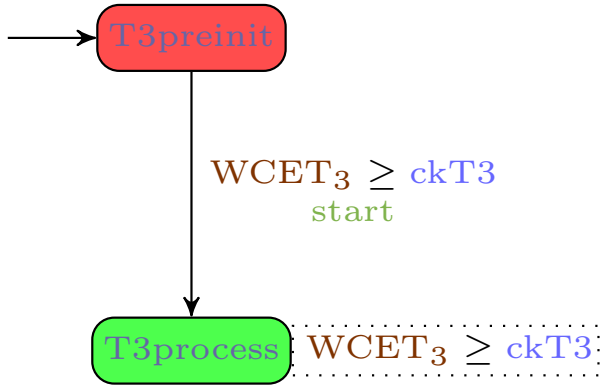


The initialization automaton

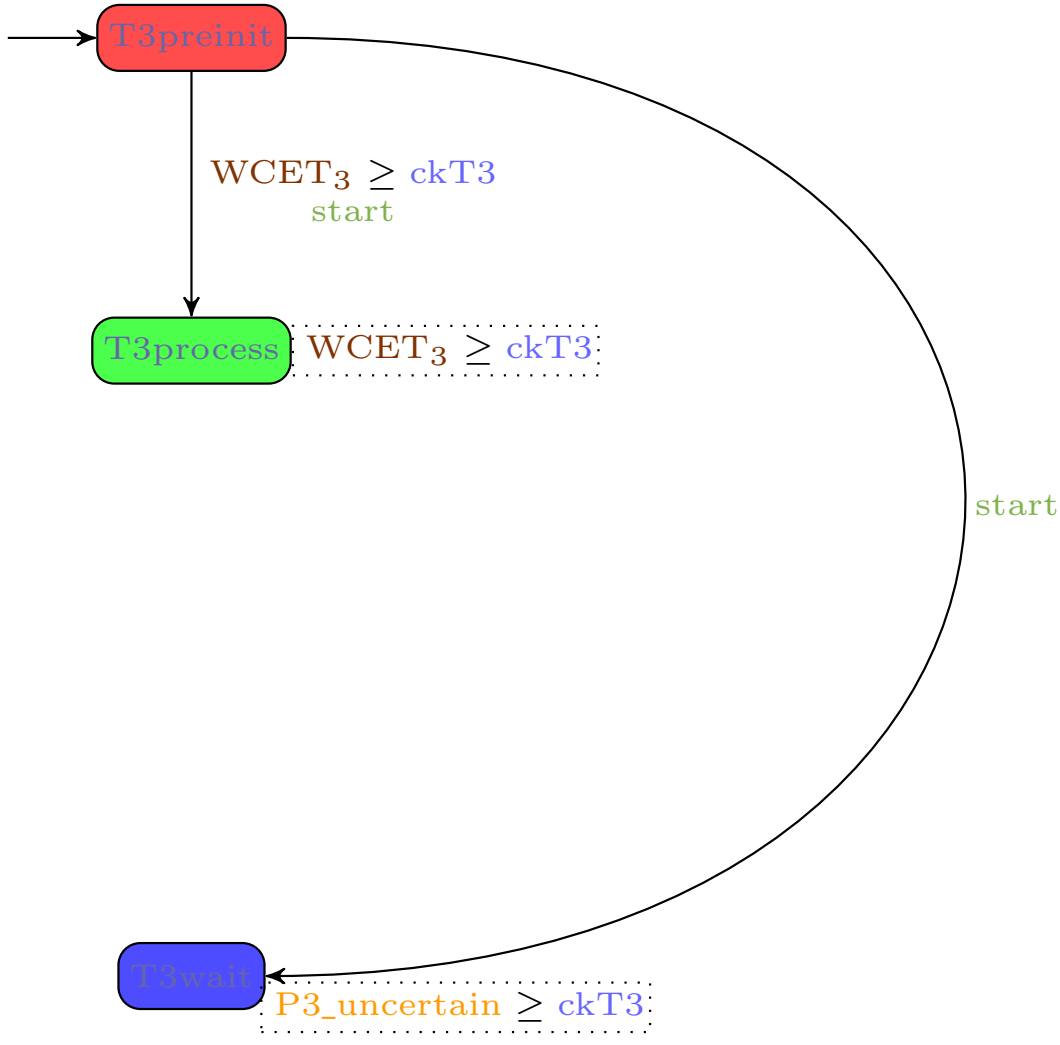


Task T3

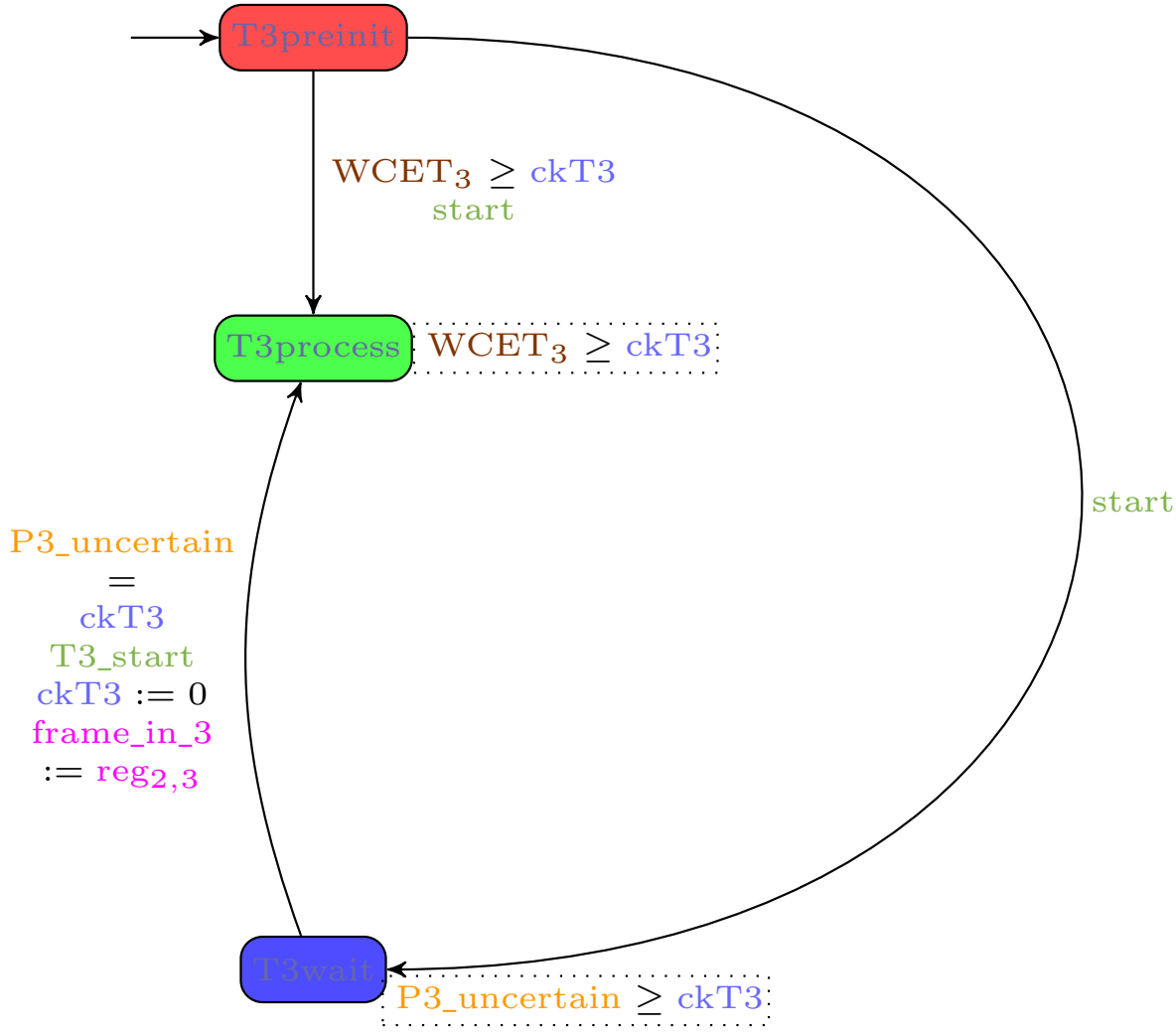
Task T3


T3preinit
$\mathrm{WCET}_3 \geq \mathrm{ckT3}$
start
T3process
$\mathrm{WCET}_3 \geq \mathrm{ckT3}$

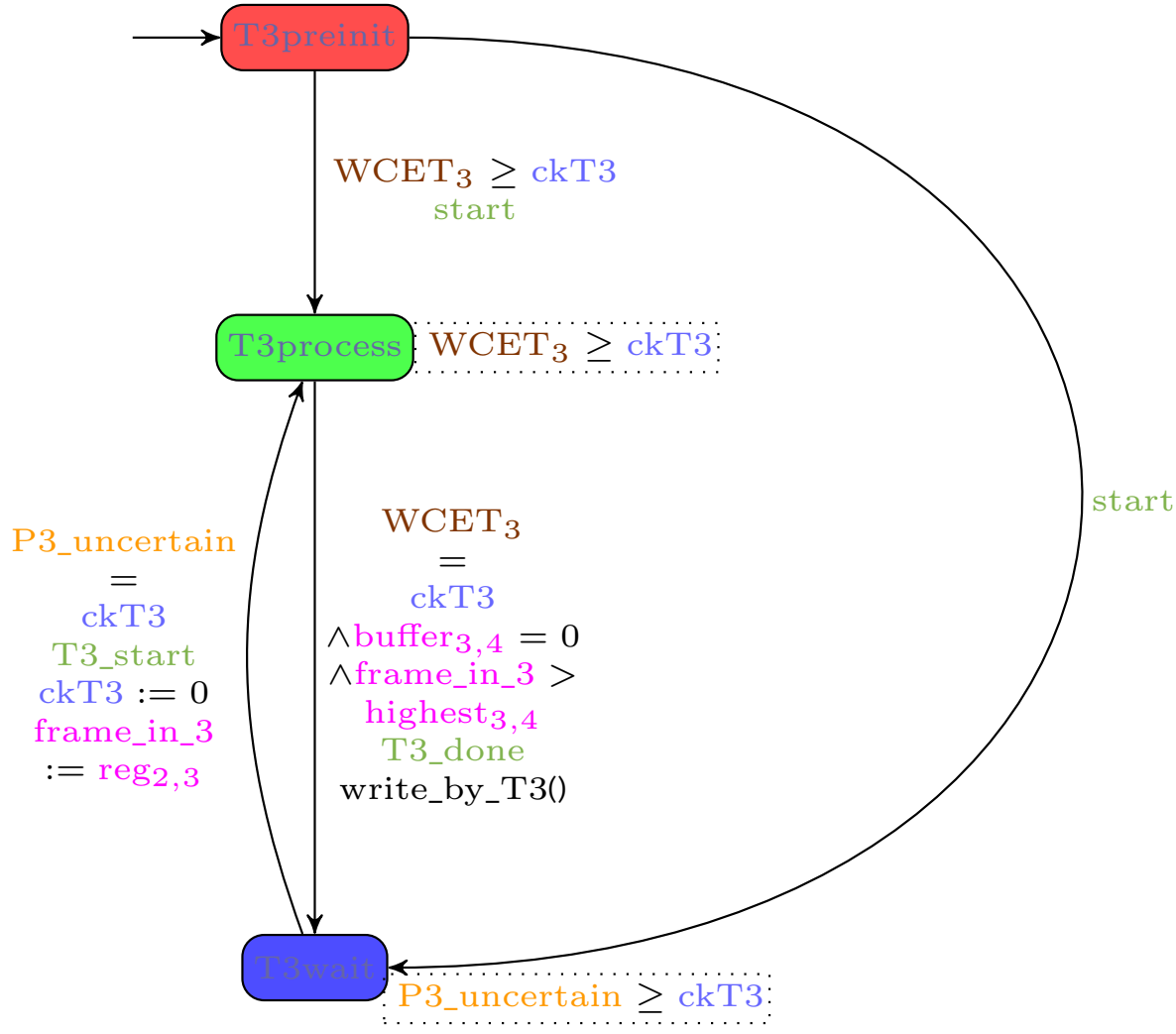
Task T3


T3preinit
$WCET_3 \geq ckT3$
start
T3process
$WCET_3 \geq ckT3$
start
T3wait
$P3\_uncertain \geq ckT3$

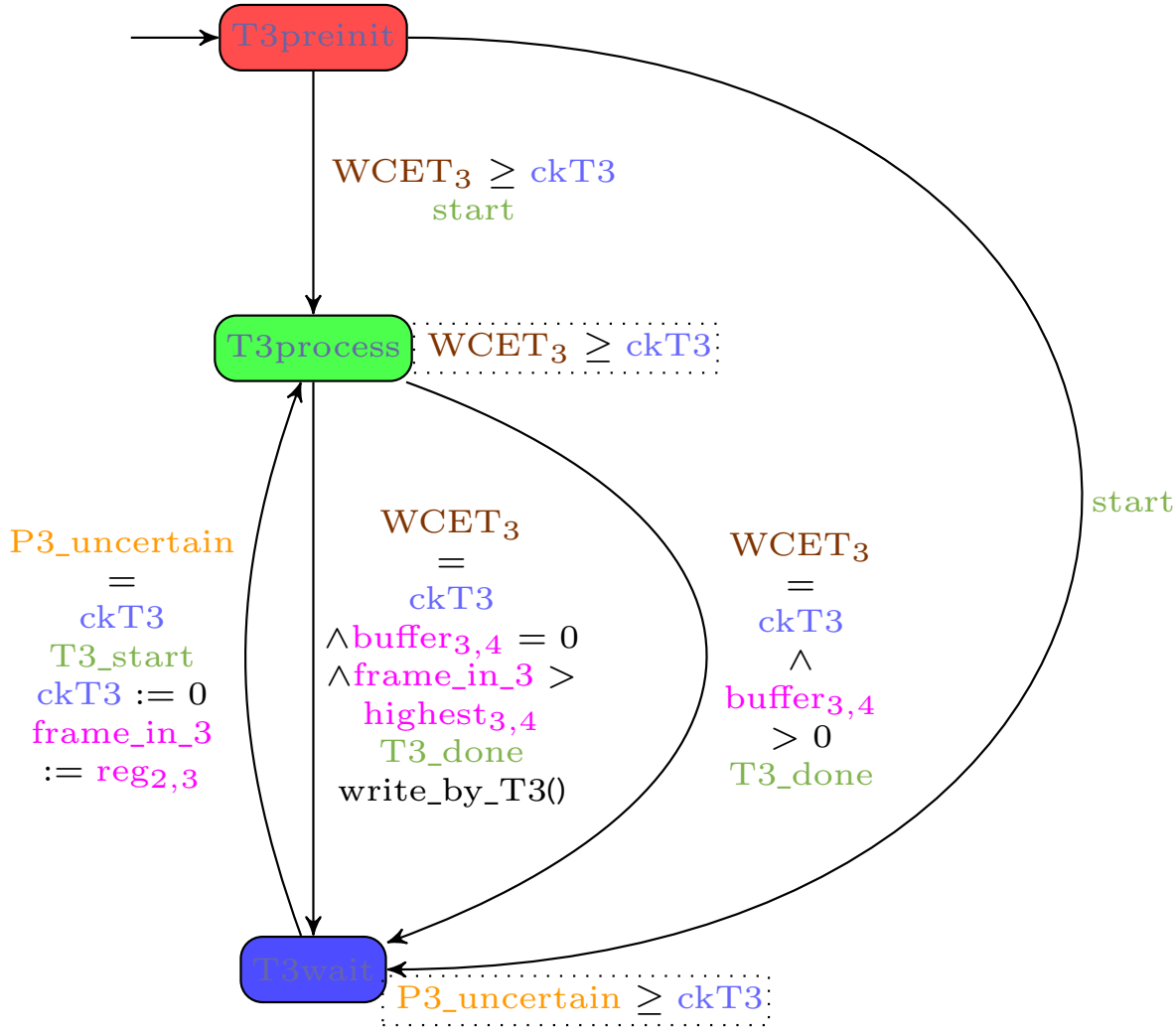
Task T3


T3preinit
WCET3 ≥ ckT3
start
T3process
WCET3 ≥ ckT3
start
P3_uncertain
=
ckT3
T3_start
ckT3 := 0
frame_in_3
:= reg2,3
T3wait
P3_uncertain ≥ ckT3

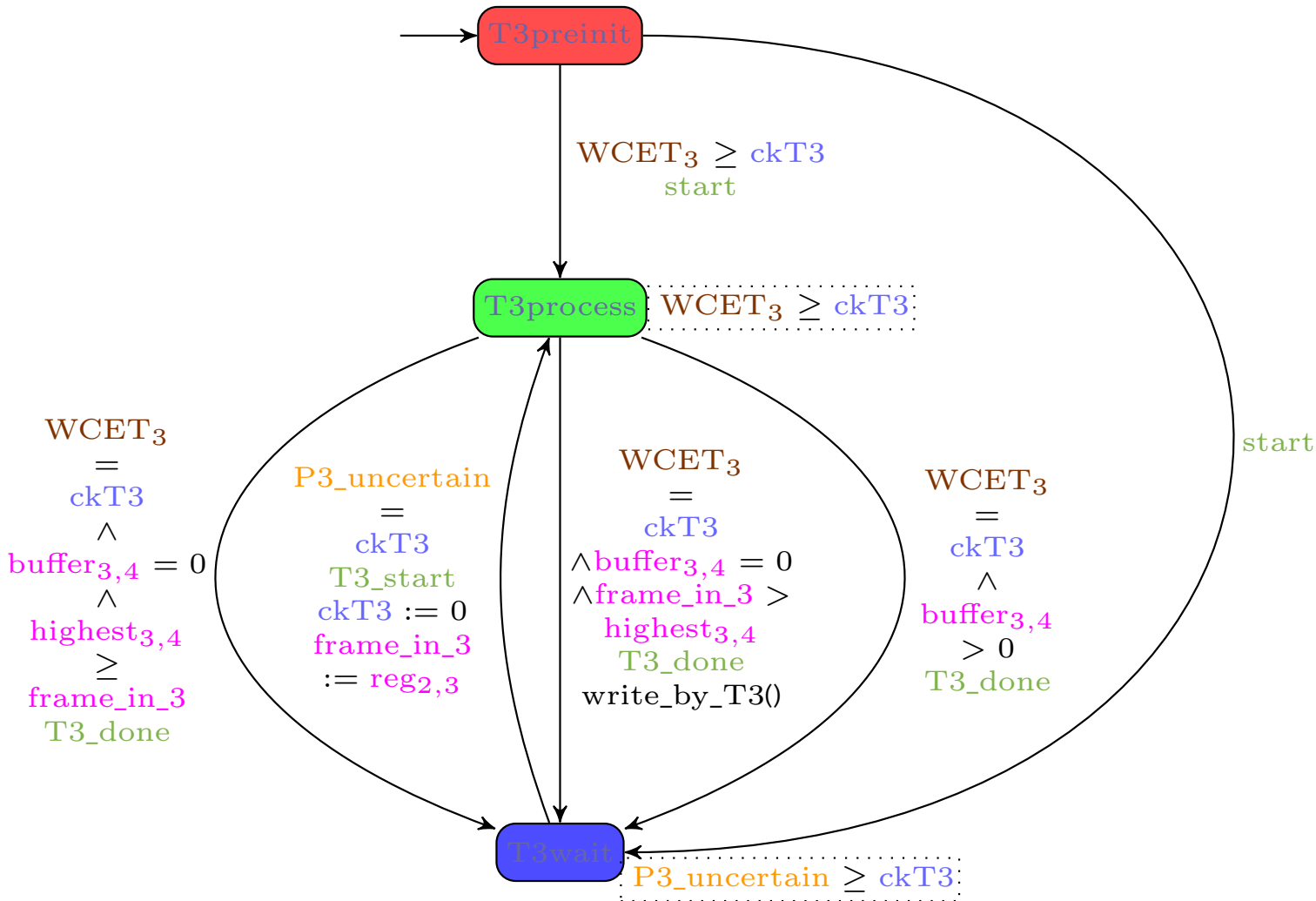
Task T3


T3preinit
WCET3 ≥ ckT3
start
T3process
WCET3 ≥ ckT3
start
P3_uncertain
=
ckT3
T3_start
ckT3 := 0
frame_in_3
:= reg2,3
WCET3
=
ckT3
∧buffer3,4 = 0
∧frame_in_3 >
highest3,4
T3_done
write_by_T3()
T3wait
P3_uncertain ≥ ckT3

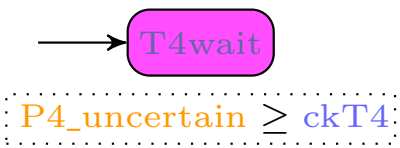
Task T3


T3preinit
WCET3 ≥ ckT3
start
T3process
WCET3 ≥ ckT3
start
P3_uncertain
=
ckT3
T3_start
ckT3 := 0
frame_in_3
:= reg2,3
WCET3
=
ckT3
∧buffer3,4 = 0
∧frame_in_3 >
highest3,4
T3_done
write_by_T3()
WCET3
=
ckT3
∧
buffer3,4
> 0
T3_done
T3wait
P3_uncertain ≥ ckT3

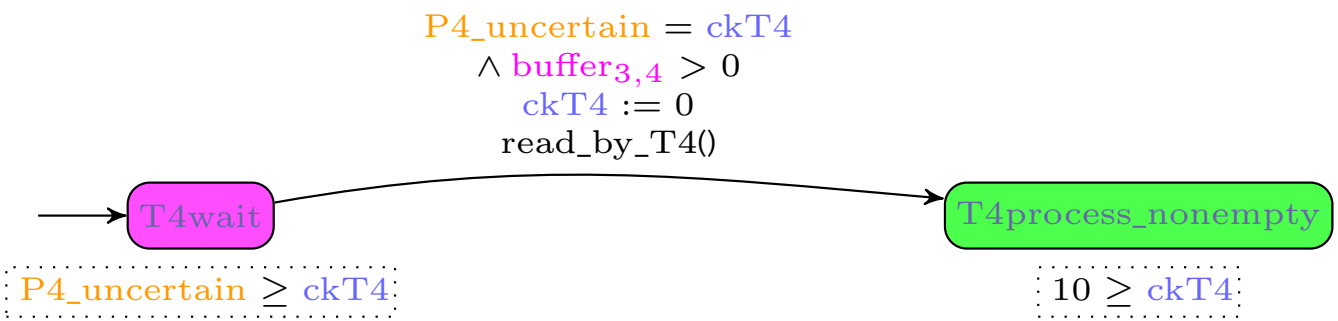
Task T3


T3preinit
WCET3 ≥ ckT3
start
T3process
WCET3 ≥ ckT3
WCET3
=
ckT3
∧
buffer3,4 = 0
∧
highest3,4
≥
frame_in_3
T3_done
P3_uncertain
=
ckT3
T3_start
ckT3 := 0
frame_in_3
:= reg2,3
WCET3
=
ckT3
∧buffer3,4 = 0
∧frame_in_3 >
highest3,4
T3_done
write_by_T3()
WCET3
=
ckT3
∧
buffer3,4
> 0
T3_done
start
T3wait
P3_uncertain ≥ ckT3

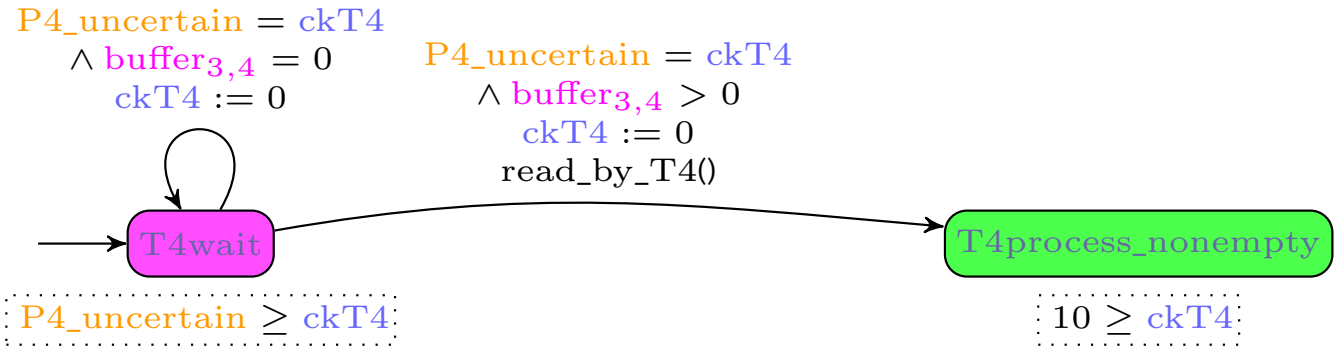
Task T4



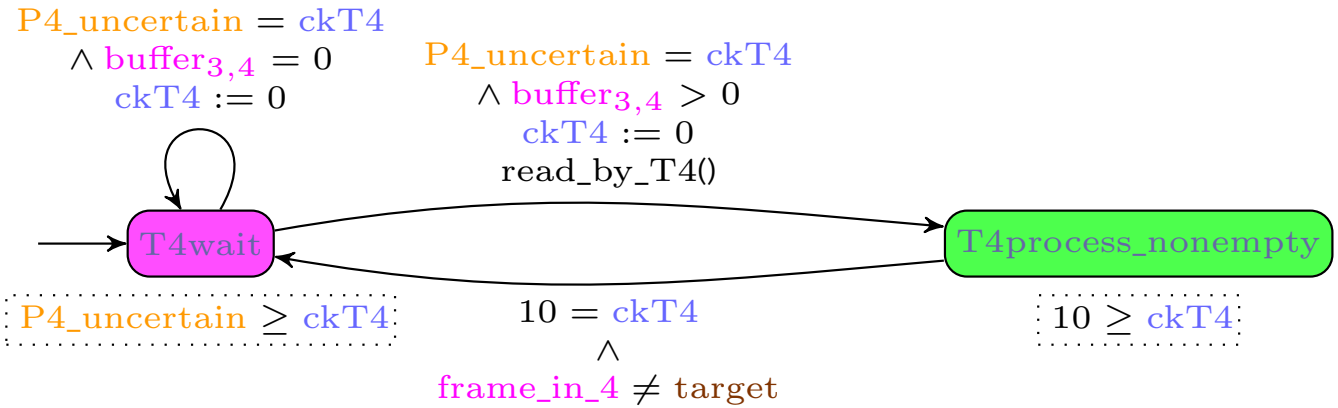
Task T4


P4_uncertain = ckT4
∧ buffer3,4 > 0
ckT4 := 0
read_by_T4()
T4wait
T4process_nonempty
P4_uncertain ≥ ckT4
10 ≥ ckT4

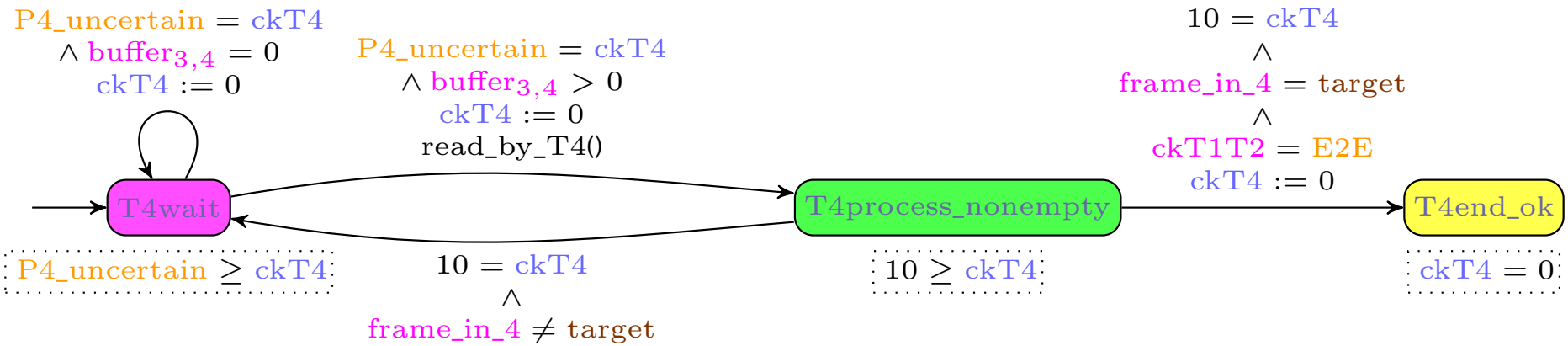
Task T4


P4_uncertain = ckT4
∧ buffer3,4 = 0
ckT4 := 0
P4_uncertain = ckT4
∧ buffer3,4 > 0
ckT4 := 0
read_by_T4()
T4wait
T4process_nonempty
P4_uncertain ≥ ckT4
10 ≥ ckT4

Task T4


P4_uncertain = ckT4
∧ buffer3,4 = 0
ckT4 := 0
P4_uncertain = ckT4
∧ buffer3,4 > 0
ckT4 := 0
read_by_T4()
T4wait
T4process_nonempty
P4_uncertain ≥ ckT4
10 = ckT4
∧
frame_in_4 ≠ target
10 ≥ ckT4

Task T4


P4_uncertain = ckT4
∧ buffer3,4 = 0
ckT4 := 0
P4_uncertain = ckT4
∧ buffer3,4 > 0
ckT4 := 0
read_by_T4()
10 = ckT4
∧
frame_in_4 = target
∧
ckT1T2 = E2E
ckT4 := 0
T4wait
T4process_nonempty
T4end_ok
P4_uncertain ≥ ckT4
10 = ckT4
∧
frame_in_4 ≠ target
10 ≥ ckT4
ckT4 = 0

Results

E2E latency results for $n = 1$ and $n = 3$

	$n = 1$	$n = 3$
min E2E	63 ms	63 ms
max E2E	145.008 ms	225.016 ms

Results obtained using IMITATOR in a few seconds

[ÉA, Lipari, Sun @ WATERS'15]

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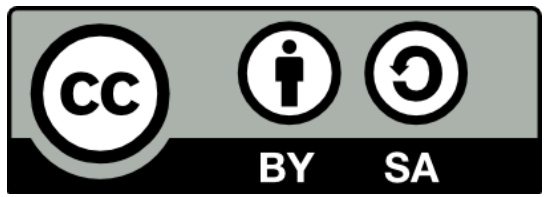
Author: **Étienne André**



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