SLAF14_3.imi

Generated by IMITATOR 3.4-beta "Cheese Durian"
Build: develop/6908f3d
Generation time: Tue Jun 23, 2024 09:33:28

t3 clocks			
t1_c t1_d t1_urgent t1_arr_x t2_c t2_d t2_urgent t2_arr_x t3_c t3_d t3_urgent t3_arr_x CPU1_urgent	2 parameters t2_D t2_arr_P	3 discrete t1_inst t2_inst t3_inst	Initial t2_arr_P >= 20 & t2_D >= 20 & 100 >= t2_D & 100 >= t2_arr_P & t1_d = 0 & t2_d = 0 & t2_arr_P = t2_arr_x & t2_urgent = 0 & t2_d = 0 & t2_c = 0 & t1_arr_x = 40 & t1_urgent = 0 & t1_d = 0 & t1_c = 0 & t3_arr_x = 100 & t3_urgent = 0 & CPU1_urgent = 0

Task_t1

t1_loc_idle | True

t1_arr_event
t1_urgent := 0;

t1_loc_act_event | 0 >= t1_urgent

t1_urgent = 0
t1_arr
t1_c := 0; t1_d := 0; t1_inst := 1;

t1_loc_act | 40 >= t1_d
stop t1_c

t1_inst < 5
t1_arr_event

t1_inst < 5
t1_arr_event
t1_inst := t1_inst + 1; t1_d := 0;

t1_dis

t1_d >= 40
t1_miss

t1_inst = 5
t1_arr_event

t1_loc_exe | 40 >= t1_d
& 5*t1_inst >= t1_c

t1_inst < 5
t1_arr_event

t1_inst < 5
t1_arr_event
t1_inst := t1_inst + 1; t1_d := 0;

t1_d >= 40
& 5*t1_inst >= t1_c
t1_miss

t1_inst = 5
t1_arr_event

t1_c = 5*t1_inst
t1_end

t1_loc_miss | True

Periodic_t1_arr

t1_arr_loc_arr | 40 >= t1_arr_x

t1_arr_x = 40
t1_arr_event
t1_arr_x := 0;

Task_t2

t2_loc_idle | True

t2_arr_event
t2_urgent := 0;

t2_loc_act_event | 0 >= t2_urgent

t2_urgent = 0
t2_arr
t2_c := 0; t2_d := 0; t2_inst := 1;

t2_loc_act | t2_D >= t2_d
stop t2_c

t2_inst < 5
t2_arr_event

t2_inst < 5
t2_arr_event
t2_inst := t2_inst + 1; t2_d := 0;

20*t2_inst > t2_c
t2_pre

t2_dis

t2_d >= t2_D
t2_miss

t2_inst = 5
t2_arr_event

t2_loc_exe | t2_D >= t2_d
& 20*t2_inst >= t2_c

t2_inst < 5
t2_arr_event

t2_inst < 5
t2_arr_event
t2_inst := t2_inst + 1; t2_d := 0;

20*t2_inst > t2_c
& t2_d >= t2_D
t2_miss

t2_inst = 5
t2_arr_event

t2_c = 20*t2_inst
t2_end

t2_loc_miss | True

Periodic_t2_arr

t2_arr_loc_arr | t2_arr_P >= t2_arr_x

t2_arr_P = t2_arr_x
t2_arr_event
t2_arr_x := 0;

Task_t3

t3_loc_idle | True

t3_arr_event
t3_urgent := 0;

t3_loc_act_event | 0 >= t3_urgent

t3_urgent = 0
t3_arr
t3_c := 0; t3_d := 0; t3_inst := 1;

t3_loc_act | 100 >= t3_d
stop t3_c

t3_inst < 5
t3_arr_event

t3_inst < 5
t3_arr_event
t3_inst := t3_inst + 1; t3_d := 0;

30*t3_inst > t3_c
t3_pre

t3_dis

t3_d >= 100
t3_miss

t3_inst = 5
t3_arr_event

t3_loc_exe | 100 >= t3_d
& 30*t3_inst >= t3_c

t3_inst < 5
t3_arr_event

t3_inst < 5
t3_arr_event
t3_inst := t3_inst + 1; t3_d := 0;

t3_d >= 100
& 30*t3_inst > t3_c
t3_miss

t3_inst = 5
t3_arr_event

t3_c = 30*t3_inst
t3_end

t3_loc_miss | True

Periodic_t3_arr

t3_arr_loc_arr | 100 >= t3_arr_x

t3_arr_x = 100
t3_arr_event
t3_arr_x := 0;

sched_CPU1

CPU1_loc_ | True

t1_arr
CPU1_urgent := 0;

t2_arr
CPU1_urgent := 0

t3_arr
CPU1_urgent := 0;

CPU1_loc_At1 | 0 >= CPU1_urgent

CPU1_urgent = 0
t1_dis

CPU1_loc_Rt1 | True

t3_arr
CPU1_urgent := 0;

t1_end
CPU1_urgent := 0;

t2_arr
CPU1_urgent := 0;

CPU1_loc_Rt1Wt3 | True

t1_end
CPU1_urgent := 0;

t2_arr
CPU1_urgent := 0;

CPU1_loc_Et1 | 0 >= CPU1_urgent

CPU1_loc_Rt1Wt2 | True

t3_arr
CPU1_urgent := 0;

t1_end
CPU1_urgent := 0;

CPU1_loc_Et1Wt3 | 0 >= CPU1_urgent

CPU1_loc_Rt1Wt2Wt3 | True

t1_end
CPU1_urgent := 0;

CPU1_loc_Et1Wt2 | 0 >= CPU1_urgent

CPU1_urgent = 0
t2_dis

CPU1_loc_Et1Wt2Wt3 | 0 >= CPU1_urgent

CPU1_loc_Rt2 | True

t3_arr
CPU1_urgent := 0;

t2_end
CPU1_urgent := 0;

t1_arr
CPU1_urgent := 0;

CPU1_loc_Rt2Wt3 | True

t2_end
CPU1_urgent := 0;

t1_arr
CPU1_urgent := 0;

CPU1_loc_At1Rt2 | 0 >= CPU1_urgent

CPU1_loc_Et2 | 0 >= CPU1_urgent

CPU1_urgent = 0
t2_pre

CPU1_loc_Et2Wt3 | 0 >= CPU1_urgent

CPU1_loc_At1Rt2Wt3 | 0 >= CPU1_urgent

CPU1_loc_At1Wt2 | 0 >= CPU1_urgent

CPU1_urgent = 0
t3_dis

CPU1_loc_Rt3 | True

CPU1_loc_At1Wt2Wt3 | 0 >= CPU1_urgent

t1_arr
CPU1_urgent := 0;

t3_end
CPU1_urgent := 0;

t2_arr
CPU1_urgent := 0;

CPU1_loc_At1Rt3 | 0 >= CPU1_urgent

CPU1_loc_Et3 | 0 >= CPU1_urgent

CPU1_loc_At2Rt3 | 0 >= CPU1_urgent

CPU1_urgent = 0
t3_pre

CPU1_loc_At1Wt3 | 0 >= CPU1_urgent

CPU1_loc_stop | True

CPU1_loc_At2Wt3 | 0 >= CPU1_urgent

CPU1_urgent = 0
t2_dis

CPU1_urgent = 0

CPU1_loc_At2 | 0 >= CPU1_urgent

CPU1_urgent = 0
t1_dis

OBS_dline

dline_loc_nomiss | True

t1_miss
t2_miss
t3_miss

dline_loc_miss | True